



+3V/+5V, 250MHz, SOT23 ADC Buffer Amplifiers with High-Speed Disable

General Description

The MAX4285/MAX4286 single and MAX4287/MAX4288/MAX4387/MAX4388 dual ADC buffer amplifiers feature high-speed performance and single +3V supply operation. The MAX4285/MAX4286/MAX4288 and MAX4388 offer a disable feature that reduces power-supply current and places the outputs in a high-impedance state. All six devices operate from a +2.85V to +6.5V single supply or from $\pm 1.425V$ to $\pm 3.25V$ dual supplies. The common-mode input voltage range extends to the negative power-supply rail (ground in single-supply applications).

These devices require 20mA of quiescent supply current per amplifier while achieving a 250MHz -3dB bandwidth and a 350V/ μ s slew rate. The combination of an 8ns (to 0.1%) settling time, 88dBc (f = 5MHz) of SFDR, and up to 100mA output drive makes these amplifiers ideal for high-speed ADC drivers for communications and instrumentation applications. In addition, when disabled, their high output impedance makes them ideal for multiplexing applications.

The MAX4285/MAX4286 are available in space-saving 6-pin SOT23 and 8-pin SO packages. The MAX4287/MAX4387 come in 8-pin μ MAX and 8-pin SO packages, while the MAX4288/MAX4388 come in 10-pin μ MAX and 14-pin SO packages.

Applications

High-Speed ADC Drivers
Communications Equipment
Instrumentation
CCD Imaging Systems
Ultrasound

Typical Operating Circuit appears at end of data sheet.

Pin Configurations appear at end of data sheet.

Features

- ◆ **High Speed at 3V**
250MHz -3dB Bandwidth (MAX4285/87/88)
150MHz -3dB Bandwidth (MAX4286, MAX4387/88)
350V/ μ s Slew Rate
- ◆ **+2.85V to +6.5V Single-Supply Operation**
- ◆ **Input Common-Mode Range Extends to V_{EE}**
- ◆ **Low Distortion at 5MHz**
-88dBc SFDR
- ◆ **High Output Current Drive: -106mA to +77mA**
- ◆ **6ns Settling Time to 0.1%**
- ◆ **High-Speed Enable/Disable**
40ns Enable Time
50ns Disable Time
High Output Impedance
- ◆ **Space-Saving SOT23 and μ MAX Packages**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK
MAX4285 EUT-T	-40°C to +85°C	6 SOT23-6	AABQ
MAX4285ESA	-40°C to +85°C	8 SO	—
MAX4286 EUT-T	-40°C to +85°C	6 SOT23-6	AABR
MAX4286ESA	-40°C to +85°C	8 SO	—
MAX4287 EUA	-40°C to +85°C	8 μ MAX	—
MAX4287ESA	-40°C to +85°C	8 SO	—

Ordering Information continued at end of data sheet.

Selector Guide

PART	OP AMPS PER PKG	MIN GAIN	-3dB BANDWIDTH (AT MIN GAIN)	HIGH-SPEED DISABLE	PIN-PACKAGE
MAX4285	1	1	250MHz	Yes	6-pin SOT23, 8-pin SO
MAX4286	1	5	150MHz	Yes	6-pin SOT23, 8-pin SO
MAX4287	2	1	250MHz	No	8-pin μ MAX/SO
MAX4288	2	1	250MHz	Yes	10-pin μ MAX/14-pin SO
MAX4387	2	5	150MHz	No	8-pin μ MAX/SO
MAX4388	2	5	150MHz	Yes	10-pin μ MAX, 14-pin SO



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ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{CC} - V_{EE}$)-0.3V to +7.5V
 Input Voltage Range ($IN+$, $IN-$)($V_{EE} - 0.3V$) to ($V_{CC} + 0.3V$)
 Differential Input Voltage-0.3V to +7.5V
 Voltage at $\overline{DISABLE}$ ($V_{EE} - 0.3V$) to ($V_{CC} + 0.3V$)
 Current into $IN+$, $IN-$, $\overline{DISABLE}$ $\pm 20mA$
 Output Short-Circuit DurationIndefinite
 Continuous Power Dissipation ($T_A = +70^\circ C$)
 6-Pin SOT23 (derate 7.1mW/ $^\circ C$ above $+70^\circ C$).....571mW

8-Pin μMAX (derate 4.1mW/ $^\circ C$ above $+70^\circ C$)330mW
 10-Pin μMAX (derate 5.6mW/ $^\circ C$ above $+70^\circ C$)444mW
 8-Pin SO (derate 5.88mW/ $^\circ C$ above $+70^\circ C$).....471mW
 14-Pin SO (derate 8.3mW/ $^\circ C$ above $+70^\circ C$).....667mW
 Operating Temperature Range-40 $^\circ C$ to +85 $^\circ C$
 Junction Temperature+150 $^\circ C$
 Storage Temperature Range-65 $^\circ C$ to +150 $^\circ C$
 Lead Temperature (soldering, 10s)+300 $^\circ C$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

($V_{CC} = +3V$, $V_{EE} = 0$, $\overline{DISABLE} = 3V$, $R_L = \infty$, $V_{CM} = 1V$, and $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage Range		Guaranteed by PSRR test		2.85		6.5	V
Input Common-Mode Voltage Range	V_{CM}	Guaranteed by CMRR test		V_{EE}		$V_{CC} - 1.25$	V
Input Offset Voltage	V_{OS}	MAX4_87EU_/MAX4_88EU_/MAX4_8_ES_		± 0.1		± 8	mV
		MAX4285EUT-T/MAX4286EUT-T		± 1.5		± 12	
Input Offset-Voltage Temperature Coefficient	TC_{VOS}				26		$\mu V/^\circ C$
Input Offset-Voltage Matching	ΔV_{OS}	MAX4287/88 and MAX4387/88			± 0.2		mV
Input Bias Current	I_B				13	35	μA
Input Offset Current	I_{OS}				0.2	8	μA
Input Resistance	R_{IN}	Differential ($-10mV \leq V_{IN} \leq +10mV$)			38		k Ω
		Common mode ($V_{EE} \leq V_{CM} \leq V_{CC} - 1.25V$)			600		
Common-Mode Rejection Ratio	CMRR	$V_{EE} \leq V_{CM} \leq V_{CC} - 1.25V$	MAX4_87EU_/MAX4_88EU_/MAX4_8_ES_		50	73	dB
			MAX4285EUT-T/MAX4286EUT-T		45	68	
Open-Loop Gain	A_{VOL}	$V_{EE} + 0.4V \leq V_{OUT} \leq V_{CC} - 0.4V$	$R_L = 2k\Omega$	75	94		dB
			$R_L = 300\Omega$	65	94		
			$R_L = 100\Omega$	60	85		

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DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +3V$, $V_{EE} = 0$, $\overline{DISABLE}_- = 3V$, $R_L = \infty$, $V_{CM} = 1V$, and $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Current Drive	I_{OUT}	$R_L = 20\Omega$ to V_{EE}			77		mA
		$R_L = 20\Omega$ to V_{CC}			106		
Power-Supply Rejection Ratio	PSRR	$V_{CC} = 2.85V$ to $6.5V$		40	50		dB
Disabled Output Leakage Current	I_{LEAK}	$\overline{DISABLE}_- = V_{EE}$, $V_{EE} \leq V_{OUT} \leq V_{CC}$			700		nA
$\overline{DISABLE}_-$ Logic Low Threshold	V_{IL}					$V_{CC} - 2$	V
$\overline{DISABLE}_-$ Logic High Threshold	V_{IH}			$V_{CC} - 1$			V
$\overline{DISABLE}_-$ Logic Input Low Current	I_{IL}	$\overline{DISABLE}_- = V_{EE}$			± 3	± 22	μA
$\overline{DISABLE}_-$ Logic Input High Current	I_{IH}	$\overline{DISABLE}_- = V_{CC}$			± 3	± 22	μA
Quiescent Supply Current (per Amplifier)	I_{SY}	$V_{CC} = 3V$	Normal mode		20	24	mA
			Disabled mode, $\overline{DISABLE}_- = V_{EE}$		1	3	
		$V_{CC} = 5V$	Normal mode		23	28	
			Disabled mode, $\overline{DISABLE}_- = V_{EE}$		1	3	

MAX4285-MAX4288/MAX4387/MAX4388

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AC ELECTRICAL CHARACTERISTICS

($V_{CC} = +3V$, $V_{EE} = 0$, $\overline{DISABLE} = 3V$, $R_L = 300\Omega$ to $V_{CC}/2$, $V_{CM} = 1V$, $A_{VCL} = +1V/V$ for MAX4285/MAX4287/MAX4288, $A_{VCL} = +5V/V$ for MAX4286 and MAX4387/MAX4388, $T_A = +25^\circ C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Small-Signal -3dB Bandwidth	BW _{SS}	$V_{OUT} = 100mVp-p$	MAX4285/87/88		250		MHz
			MAX4286 and MAX4387/88		150		
Large-Signal -3dB Bandwidth	BW _{LS}	$V_{OUT} = 1Vp-p$			200		MHz
Bandwidth for 0.1dB Flatness	BW _{0.1dB}	$V_{OUT} = 100mVp-p$	MAX4285/87/88		100		MHz
			MAX4286 and MAX4387/88		50		
Slew Rate	SR	$V_{OUT} = 1V$ step, 10% to 90%			350		V/ μs
Rise Time	t _R	$V_{OUT} = 1V$ step, 10% to 90%			2.2		ns
Fall Time	t _F	$V_{OUT} = 1V$ step, 90% to 10%			2.8		ns
Settling Time (0.1%)	t _{s 0.1%}	$V_{OUT} = 1V$ step	MAX4285/87/88		6		ns
			MAX4286 and MAX4387/88		14		
Overload Recovery Time		10% overdrive			25		ns
Spurious-Free Dynamic Range	SFDR	$V_{OUT} = 0.5Vp-p$	f _C = 100kHz		88		dBc
			f _C = 1MHz		88		
			f _C = 5MHz		87		
			f _C = 10MHz		79		
			f _C = 20MHz		70		
			f _C = 60MHz		50		
Two-Tone Third-Order Intercept	IP ₃	f _C = 20MHz			34		dBm
Input Noise Voltage Density	e _n	f = 1MHz			10		nV/ $\sqrt{Hz}$
Input Noise Current Density	i _n	f = 1MHz			2.1		pA/ $\sqrt{Hz}$
Input Capacitance	C _{IN}				2		pF
Output Impedance	Z _{OUT}	f = 10MHz			0.5		Ω
Enable Time	t _{ON}	$V_{OUT} = 1V$, to within 0.1%			40		ns
Disable Time	t _{OFF}	$V_{OUT} = 1V$, to within 0.1%			50		
Crosstalk	X _{TALK}	MAX4287/88 and MAX4387/88, f = 10MHz, $V_{OUT} = 1Vp-p$			85		dBc

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MAX4285-MAX4288/MAX4387/MAX4388

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V, V_{EE} = 0, $\overline{\text{DISABLE}}$ = 5V, R_L = 300Ω to V_{CC}/2, V_{CM} = 2.5V, A_{vCL} = +1V/V for MAX4285/MAX4287/MAX4288, A_{vCL} = +5V/V for MAX4286 and MAX4387/MAX4388, T_A = +25°C, unless otherwise noted.)

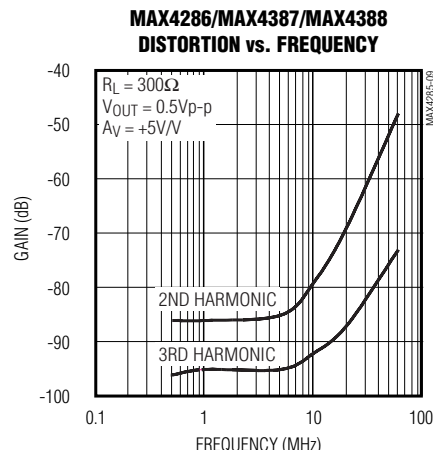
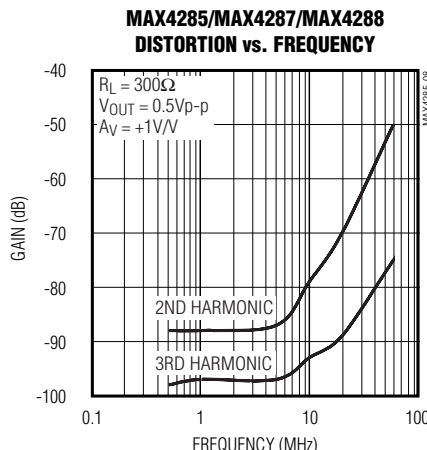
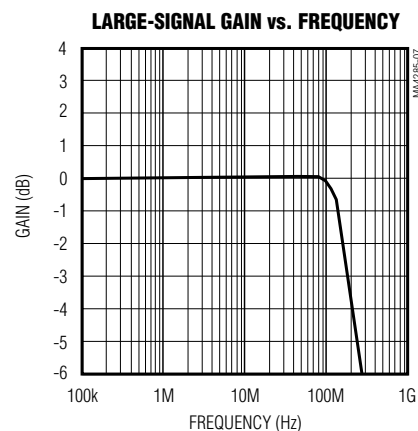
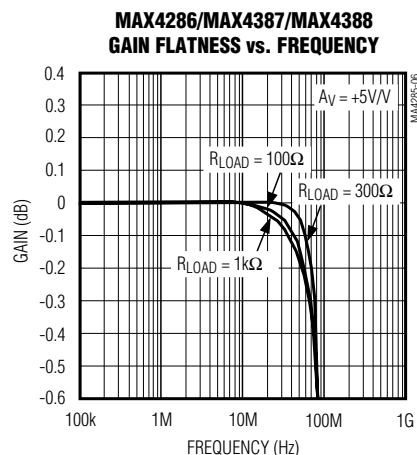
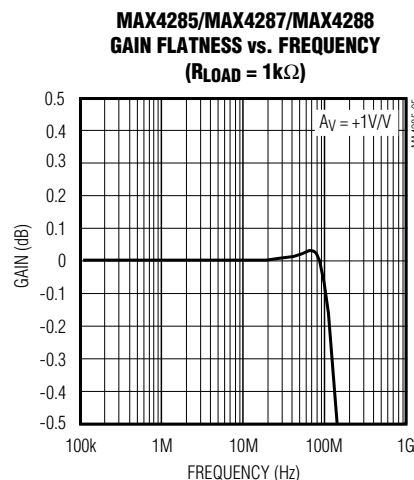
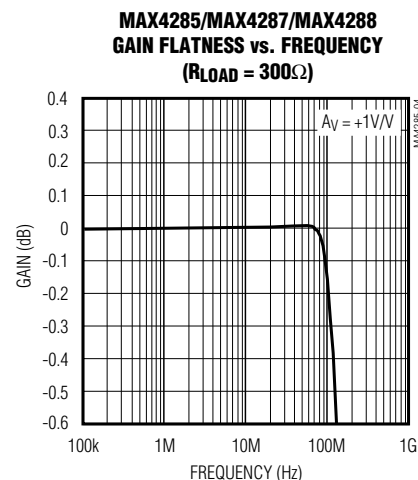
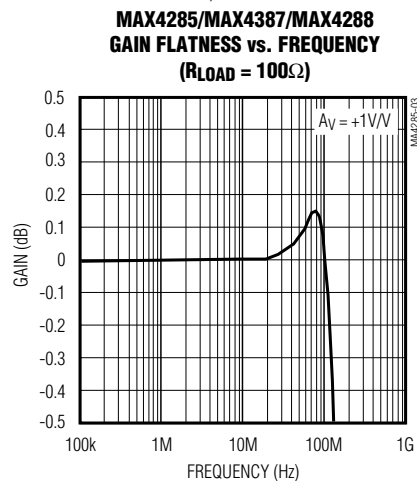
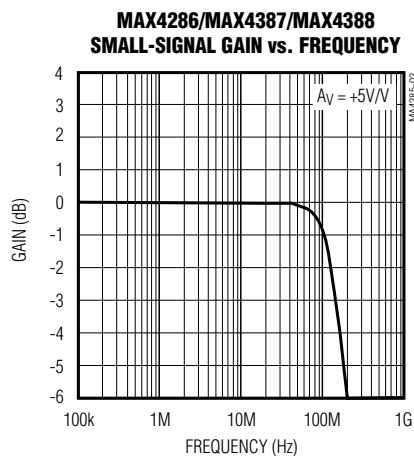
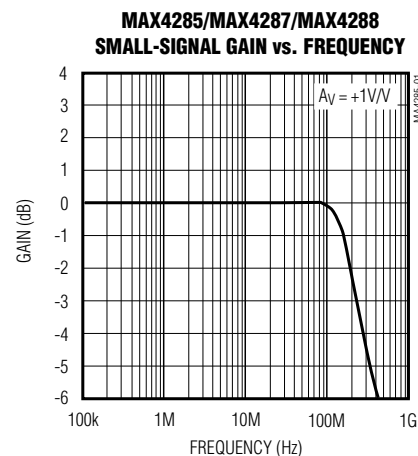
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Small-Signal -3dB Bandwidth	BW _{SS}	V _{OUT} = 100mVp-p	MAX4285/87/88		220		MHz
			MAX4286 and MAX4387/88		130		
Large-Signal -3dB Bandwidth	BW _{LS}	V _{OUT} = 1Vp-p			195		MHz
Bandwidth for 0.1dB Flatness	BW _{0.1dB}	V _{OUT} = 100mVp-p	MAX4285/87/88		75		MHz
			MAX4286 and MAX4387/88		40		
Slew Rate	SR	V _{OUT} = 2V step, 10% to 90%			385		V/μs
Rise Time	t _R	V _{OUT} = 2V step, 10% to 90%			4.2		ns
Fall Time	t _F	V _{OUT} = 2V step, 90% to 10%			2.9		ns
Settling Time (0.1%)	t _{S 0.1%}	V _{OUT} = 2V step	MAX4285/87/88		8		ns
			MAX4286 and MAX4387/88		10		
Spurious-Free Dynamic Range	SFDR	V _{OUT} = 1Vp-p	f _C = 100kHz		86		dBc
			f _C = 1MHz		86		
			f _C = 5MHz		86		
			f _C = 10MHz		77		
			f _C = 20MHz		64		
			f _C = 60MHz		45		
Two-Tone Third-Order Intercept	IP3	f _C = 20MHz			40		dBm
Input Noise Voltage Density	e _n	f = 1MHz			6.5		nV/√Hz
Input Noise Current Density	i _n	f = 1MHz			1.9		pA/√Hz
Input Capacitance	C _{IN}				2		pF
Output Impedance	Z _{OUT}	f = 10MHz			0.5		Ω
Enable Time	t _{ON}	V _{OUT} = 1V, to within 0.1%			40		ns
Disable Time	t _{OFF}	V _{OUT} = 1V, to within 0.1%			35		
Crosstalk	X _{TALK}	MAX4287/88 and MAX4387/88, f = 10MHz, V _{OUT} = 2Vp-p			85		dBc

Note 1: The MAX428_EUT (SOT23) are 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design.

+3V/+5V, 250MHz, SOT23 ADC Buffer Amplifiers with High-Speed Disable

Typical Operating Characteristics

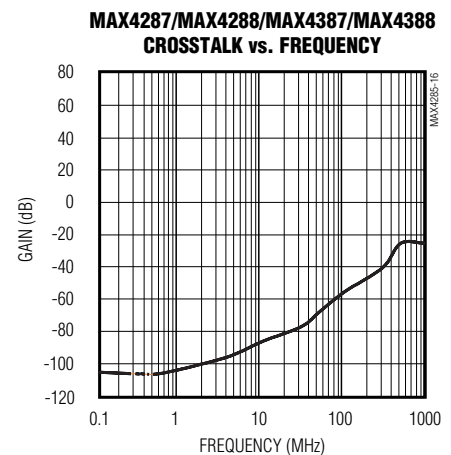
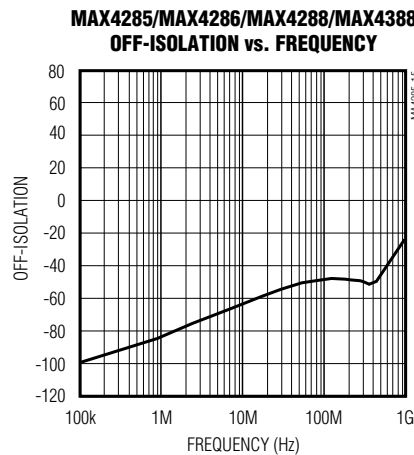
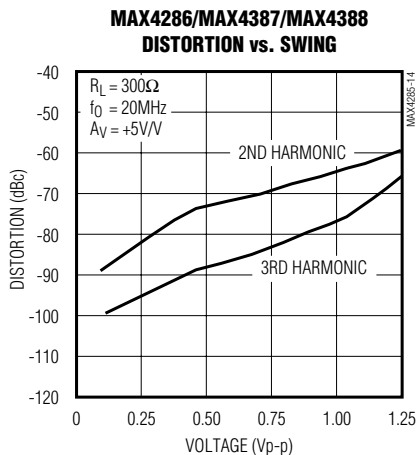
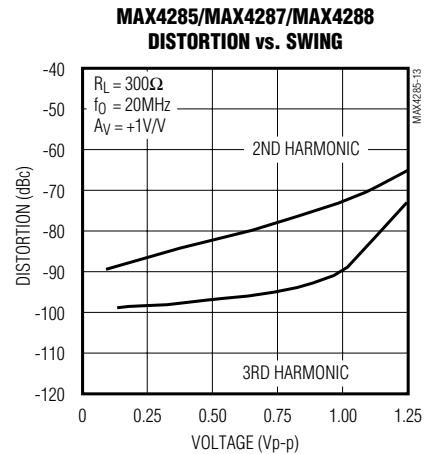
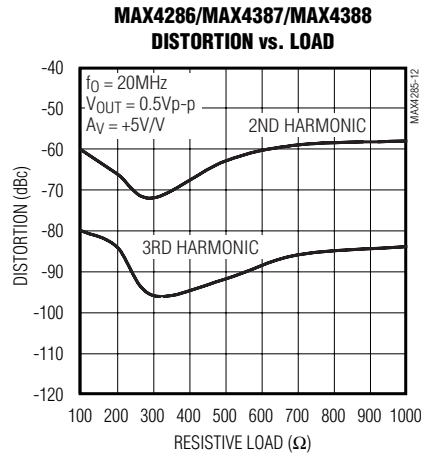
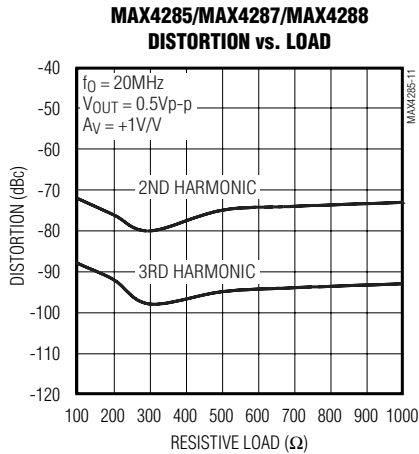
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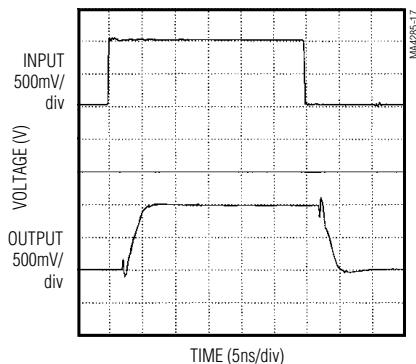
+3V/+5V, 250MHz, SOT23 ADC Buffer Amplifiers with High-Speed Disable

Typical Operating Characteristics (continued)

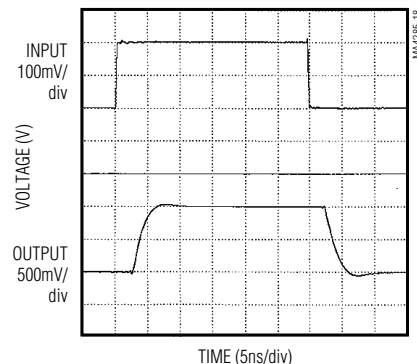
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**MAX4285/MAX4287/MAX4288
LARGE-SIGNAL PULSE RESPONSE
($A_V = +1V/V$)**



**MAX4286/MAX4387/MAX4388
LARGE-SIGNAL PULSE RESPONSE
($A_V = +5V/V$)**



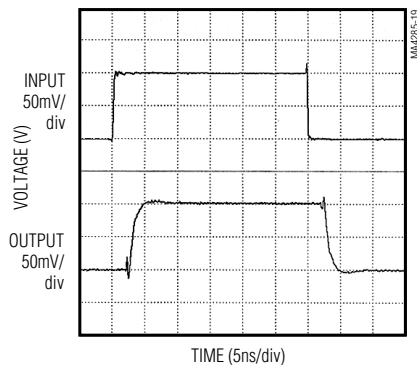
MAX4285-MAX4288/MAX4387/MAX4388

+3V/+5V, 250MHz, SOT23 ADC Buffer Amplifiers with High-Speed Disable

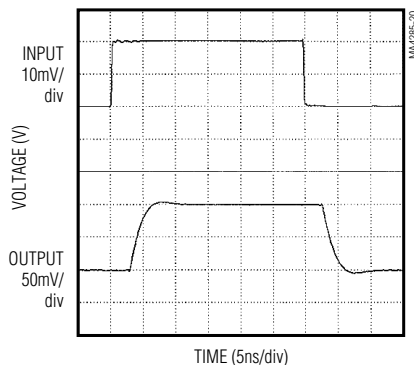
Typical Operating Characteristics (continued)

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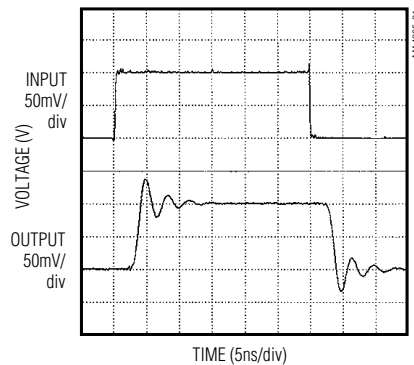
**MAX4285/MAX4287/MAX4288
SMALL-SIGNAL PULSE RESPONSE
($A_V = +1V/V$)**



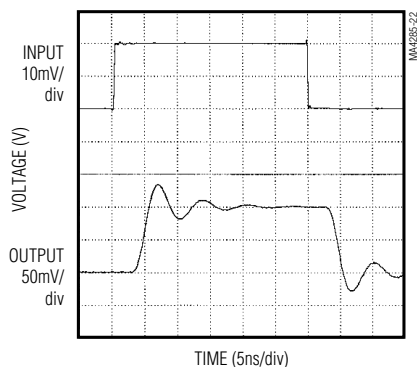
**MAX4286/MAX4387/MAX4388
SMALL-SIGNAL PULSE RESPONSE
($A_V = +5V/V$)**



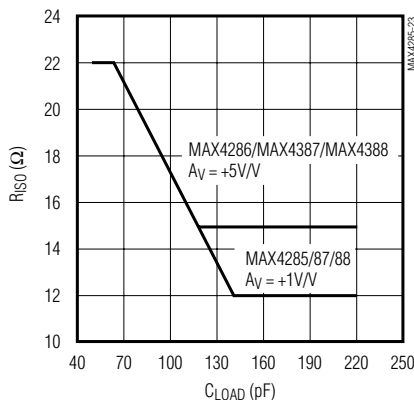
**MAX4285/MAX4287/MAX4288
SMALL-SIGNAL PULSE RESPONSE
($C_{LOAD} = 22pF$, $A_V = +1V/V$)**



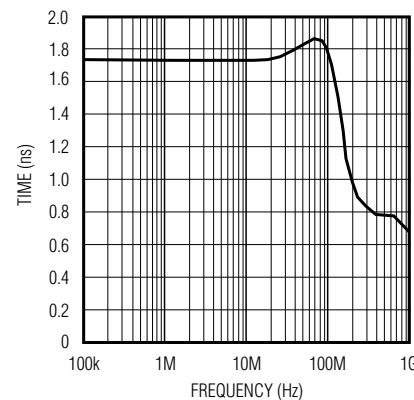
**MAX4286/MAX4387/MAX4388
SMALL-SIGNAL PULSE RESPONSE
($C_{LOAD} = 47pF$, $A_V = +5V/V$)**



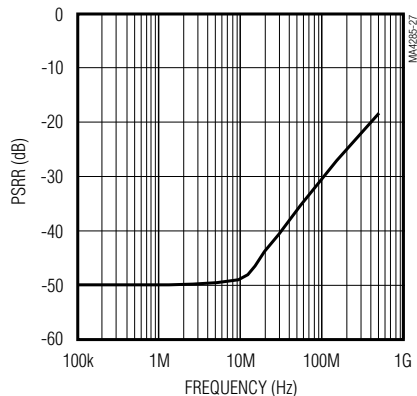
**ISOLATION RESISTANCE
vs. LOAD CAPACITANCE**



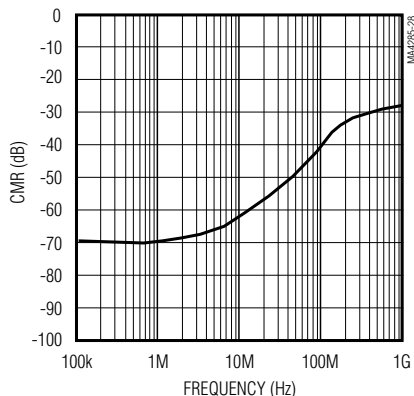
GROUP DELAY vs. FREQUENCY



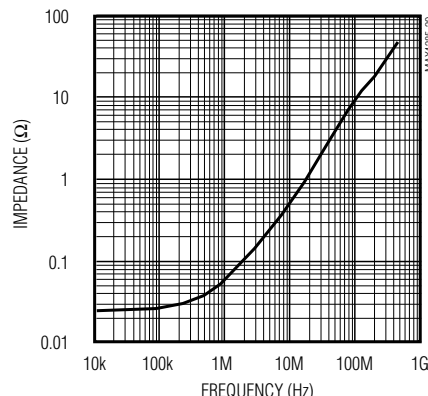
**POWER-SUPPLY REJECTION RATIO
vs. FREQUENCY**



**COMMON-MODE REJECTION
vs. FREQUENCY**



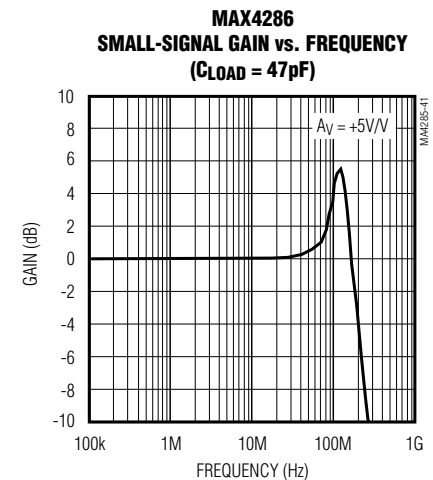
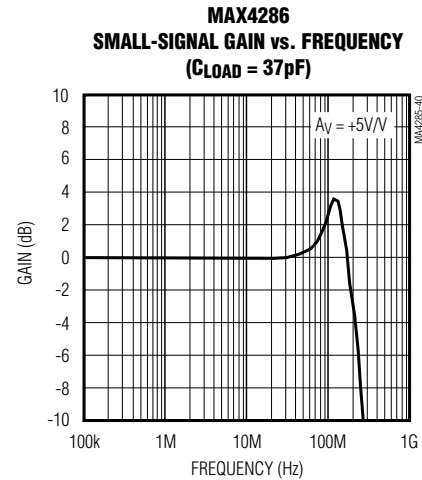
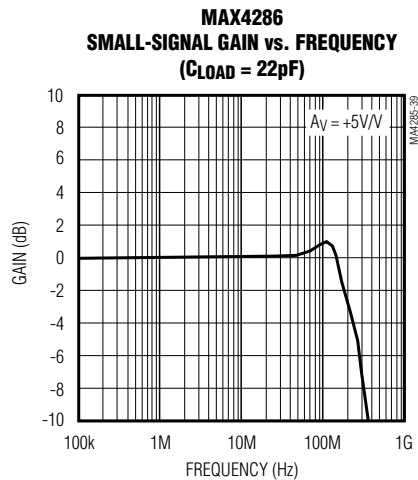
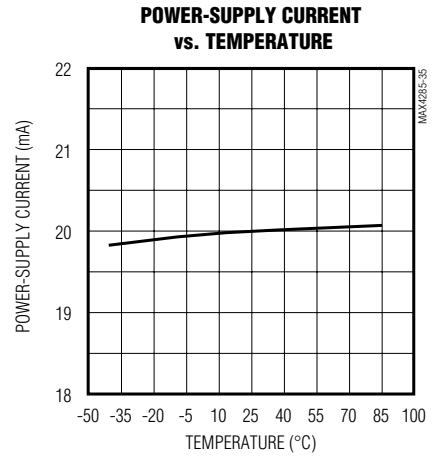
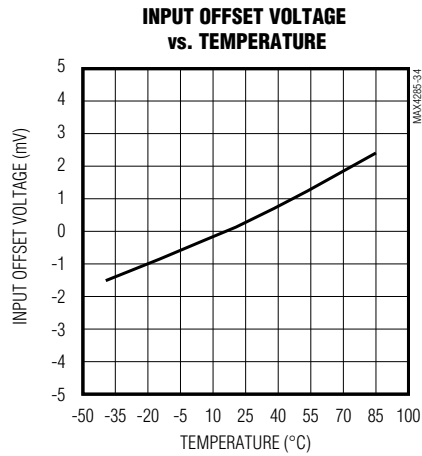
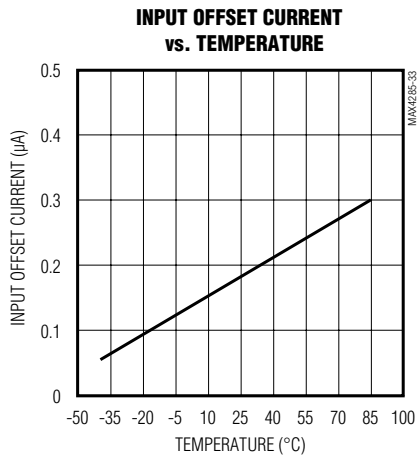
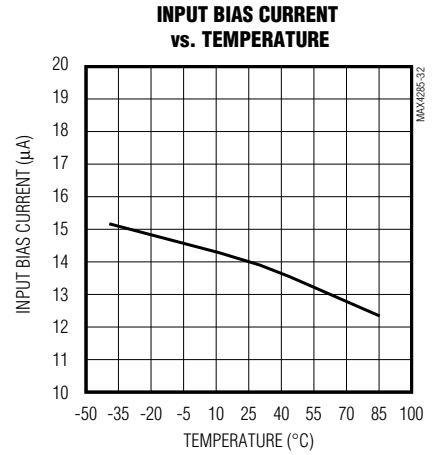
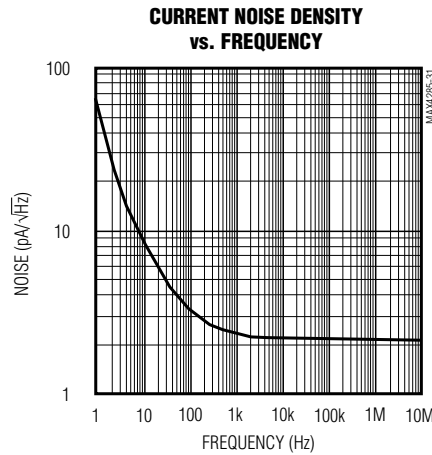
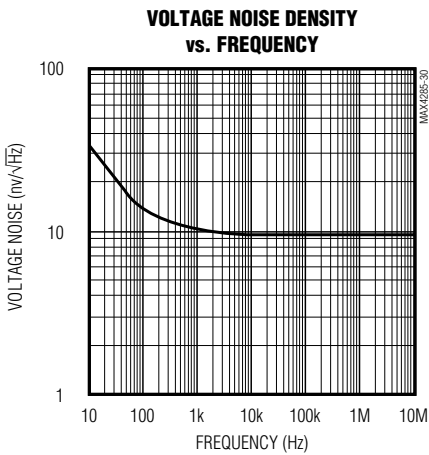
OUTPUT IMPEDANCE vs. FREQUENCY



+3V/+5V, 250MHz, SOT23 ADC Buffer Amplifiers with High-Speed Disable

Typical Operating Characteristics (continued)

($V_{CC} = +3V$, $V_{EE} = 0$, $\overline{DISABLE} \geq 2V$, $R_L = 300\Omega$ to $V_{CC}/2$, $V_{CM} = +1.0V$, $T_A = +25^\circ C$, unless otherwise noted.)

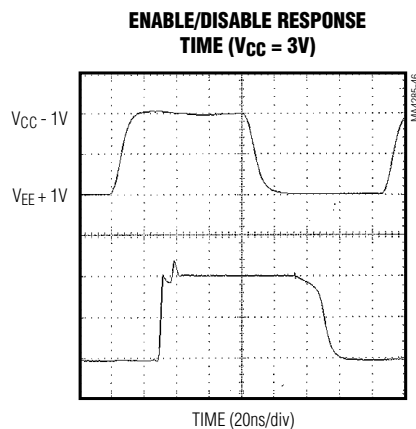
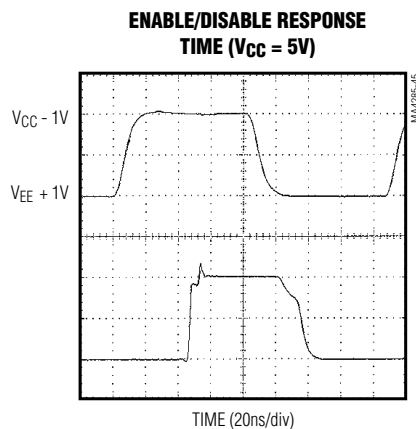
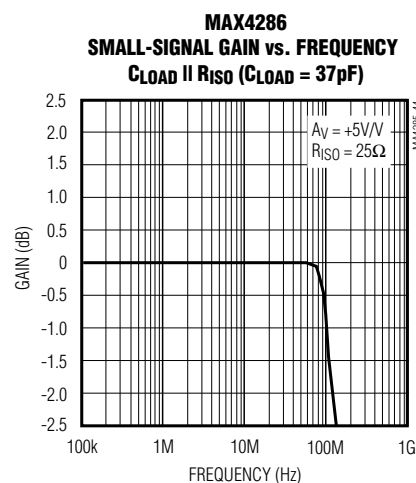
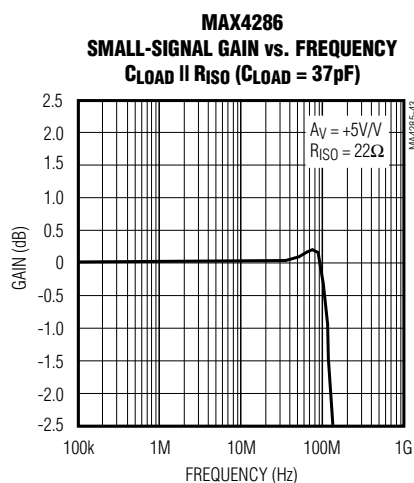
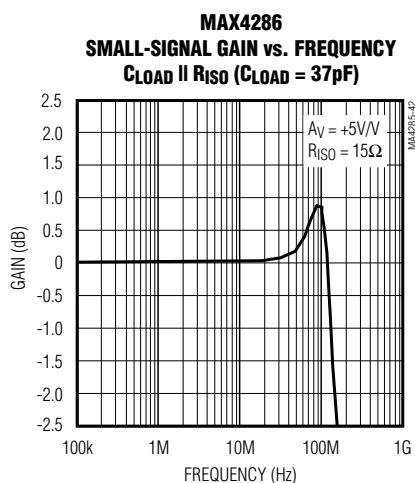


MAX4285-MAX4288/MAX4387/MAX4388

+3V/+5V, 250MHz, SOT23 ADC Buffer Amplifiers with High-Speed Disable

Typical Operating Characteristics (continued)

($V_{CC} = +3V$, $V_{EE} = 0$, $\overline{DISABLE} \geq 2V$, $R_L = 300\Omega$ to $V_{CC}/2$, $V_{CM} = +1.0V$, $T_A = +25^\circ C$, unless otherwise noted.)



+3V/+5V, 250MHz, SOT23 ADC Buffer Amplifiers with High-Speed Disable

Pin Description

PIN					NAME	FUNCTION
MAX4285 MAX4286		MAX4287 MAX4387	MAX4288 MAX4388			
6-PIN SOT23-6	8-PIN SO	8-PIN μMAX/SO	10-PIN μMAX	14-PIN SO		
—	1, 5	—	—	5, 7, 8, 10	N.C.	Not Internally Connected. Connect to ground or leave unconnected.
1	6	—	—	—	OUT	Amplifier Output
2	4	4	4	4	V _{EE}	Negative Power Supply, or Ground in Single-Supply Operation
3	3	—	—	—	IN+	Noninverting Input
4	2	—	—	—	IN-	Inverting Input
5	8	—	—	—	$\overline{\text{DISABLE}}$	Disable (active low)
—	—	—	5	6	$\overline{\text{DISABLEA}}$	Disable Amplifier A (active low)
—	—	—	6	9	$\overline{\text{DISABLEB}}$	Disable Amplifier B (active low)
6	7	8	10	14	V _{CC}	Positive Power Supply
—	—	1	1	1	OUTA	Amplifier A Output
—	—	2	2	2	INA-	Amplifier A Inverting Input
—	—	3	3	3	INA+	Amplifier A Noninverting Input
—	—	5	7	11	INB+	Amplifier B Noninverting Input
—	—	6	8	12	INB-	Amplifier B Inverting Input
—	—	7	9	13	OUTB	Amplifier B Output

Detailed Description

The MAX4285–MAX4288 and MAX4387/MAX4388 are voltage-feedback op amps, intended for use as ADC input buffers. They operate from a single +2.85V to +6.5V supply or dual $\pm 1.425\text{V}$ to $\pm 3.25\text{V}$ supplies. Their high output drive, wide bandwidth, fast settling, low noise, and low distortion make them ideal for the brutal task of meeting the dynamic input drive requirements of high-speed ADCs or other demanding applications.

The MAX4285/MAX4286/MAX4288 and MAX4388 have a high-speed disable mode that places the outputs in a high-impedance state and lowers operating supply current to 1mA. The enable time is typically 40ns, and the disable time is typically 50ns. The MAX4285/MAX4286 have a single enable pin ($\overline{\text{DISABLE}}$), and the MAX4288/

MAX4388 have dual disable pins ($\overline{\text{DISABLEA}}$, $\overline{\text{DISABLEB}}$).

The MAX4285/MAX4287/MAX4288 are internally compensated for unity-gain stability. The MAX4286/MAX4387/MAX4388 are compensated for gains of +5V/V or greater.

Applications Information

Inverting and Noninverting Configurations

Select the gain-setting feedback (R_F) and input (R_G) resistor values considering the following criteria: large resistor values increase voltage noise and interact with the amplifier's input and PC board capacitance to effect system bandwidth. This generates undesirable poles and zeros that decrease bandwidth or cause oscillations.

+3V/+5V, 250MHz, SOT23 ADC Buffer Amplifiers with High-Speed Disable

For example, a noninverting gain-of-two configuration ($R_F = R_G$) using $1k\Omega$ resistors, combined with $2pF$ typical amplifier input capacitance, generates a pole at $159MHz$. Since this pole is within the amplifier bandwidth, it jeopardizes stability. Reducing these $1k\Omega$ resistors to 100Ω extends the pole frequency to $1.59GHz$, but affects output swing by adding 200Ω in parallel with the amplifier's load resistor. The typical value for R_F is 300Ω .

Layout and Power-Supply Bypassing

These amplifiers operate from a single $+2.85V$ to $+6.5V$ power supply or from $\pm 1.425V$ to $\pm 3.25V$ dual supplies. For single-supply operation, bypass V_{CC} to ground with a $0.1nF$ capacitor as close to the pin as possible, with a $0.1\mu F$ capacitor in parallel. If operating with dual supplies, bypass each supply with capacitors to ground.

Observe the following guidelines:

- A solid ground plane is essential for good high-frequency behavior.
- Where possible, use multiple ground vias.
- Use a PC board with at least two layers. Avoid areas of unreferenced copper-clad.
- Keep signal traces as short and as straight as possible. Do not make sharp turns; round all trace corners.
- Use a constant-impedance board design if possible.

High-Speed Disable

The MAX4285/MAX4286/MAX4288 and MAX4388 feature a disable ($\overline{DISABLE}$) input that places the amplifier in a low-power, high-output-impedance state. When $\overline{DISABLE}$ is asserted, the amplifier's output impedance is typically $35k\Omega$. This high output impedance, combined with the low $2pF$ output capacitance, make these devices ideal for ADC input multiplexing applications or switch applications. Typical enable/disable times are $40ns/50ns$.

Output Capacitive Loading and Stability

These op amps are optimized for AC performance. They are not designed to drive highly reactive loads, which decrease phase margin and may produce excessive ringing and oscillation. A small isolation resistor (usually 20Ω to 30Ω) placed before the reactive load reduces possible ringing and oscillation (Figure 1). At higher capacitive loads, AC performance is dependent on the interaction of the load capacitance, the isolation resistor, and on-board layout.

Output Drive Capability

The MAX4285-MAX4288 and MAX4387/MAX4388 have an output sink capability of $106mA$ and a source capability of $77mA$. This high current ability allows them to drive low-impedance and dynamic-impedance ADC inputs. The linear output range of these devices is $(V_{EE} + 0.4V)$ to $(V_{CC} - 0.4V)$. Operation beyond this range is not recommended due to reduced gain and phase margin.

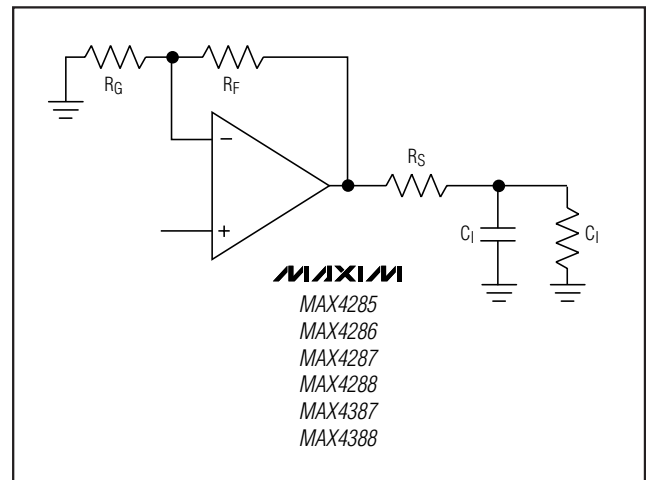


Figure 1. Using an Isolation Resistor (R_S) for High Capacitive Loads

+3V/+5V, 250MHz, SOT23 ADC Buffer Amplifiers with High-Speed Disable

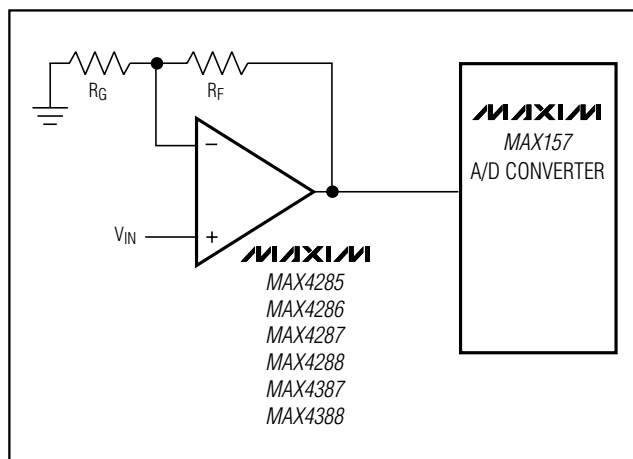
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK
MAX4288EUB	-40°C to +85°C	10 μ MAX	—
MAX4288ESD	-40°C to +85°C	14 SO	—
MAX4387EUA	-40°C to +85°C	8 μ MAX	—
MAX4387ESA	-40°C to +85°C	8 SO	—
MAX4388EUB	-40°C to +85°C	10 μ MAX	—
MAX4388ESD	-40°C to +85°C	14 SO	—

Chip Information

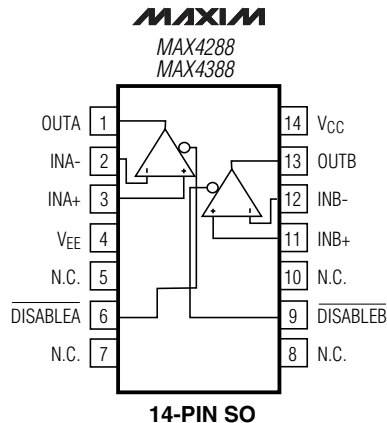
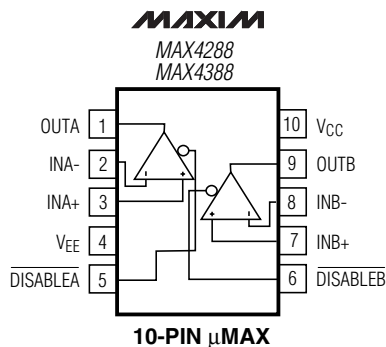
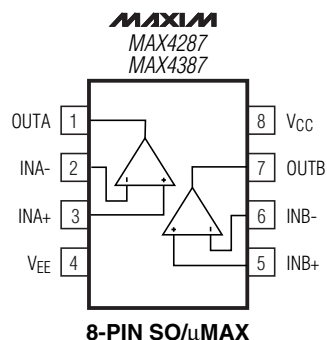
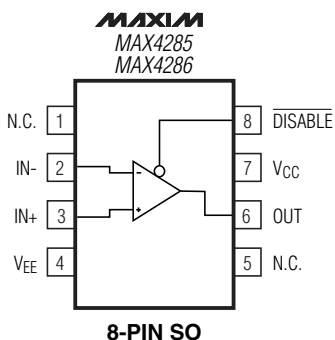
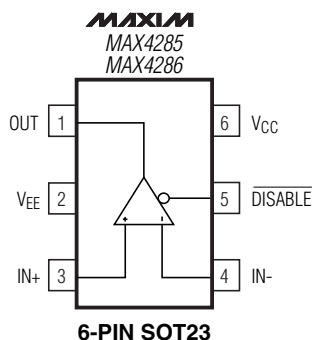
TRANSISTOR COUNT: MAX4285/MAX4286 : 114
 MAX4287/MAX4288/
 MAX4387/MAX4388 : 227

Typical Operating Circuit



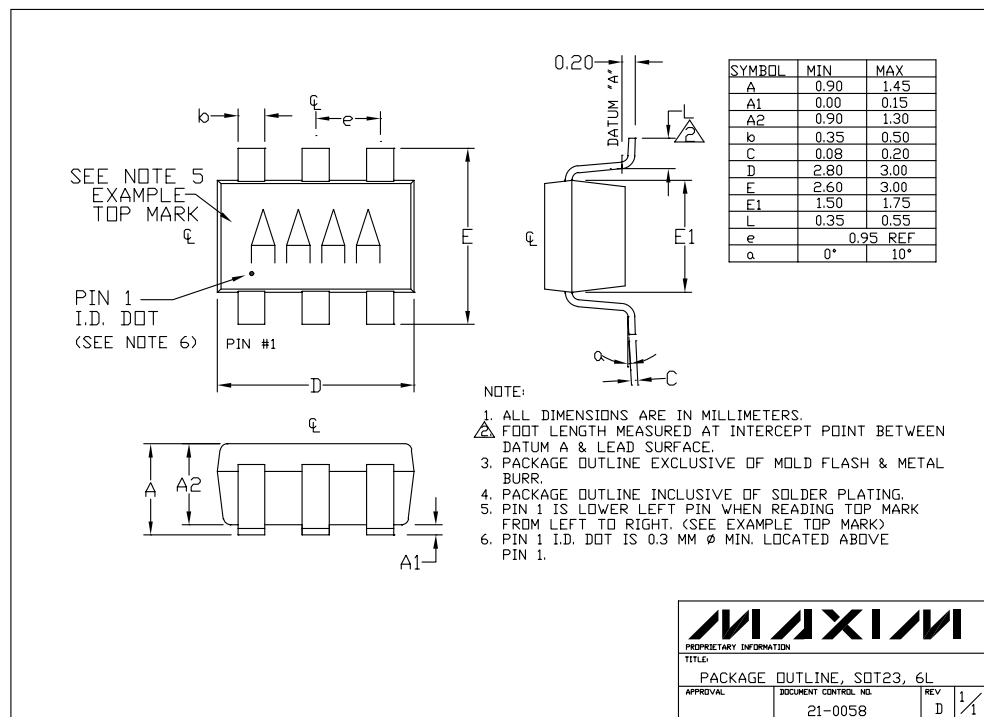
Pin Configurations

TOP VIEW

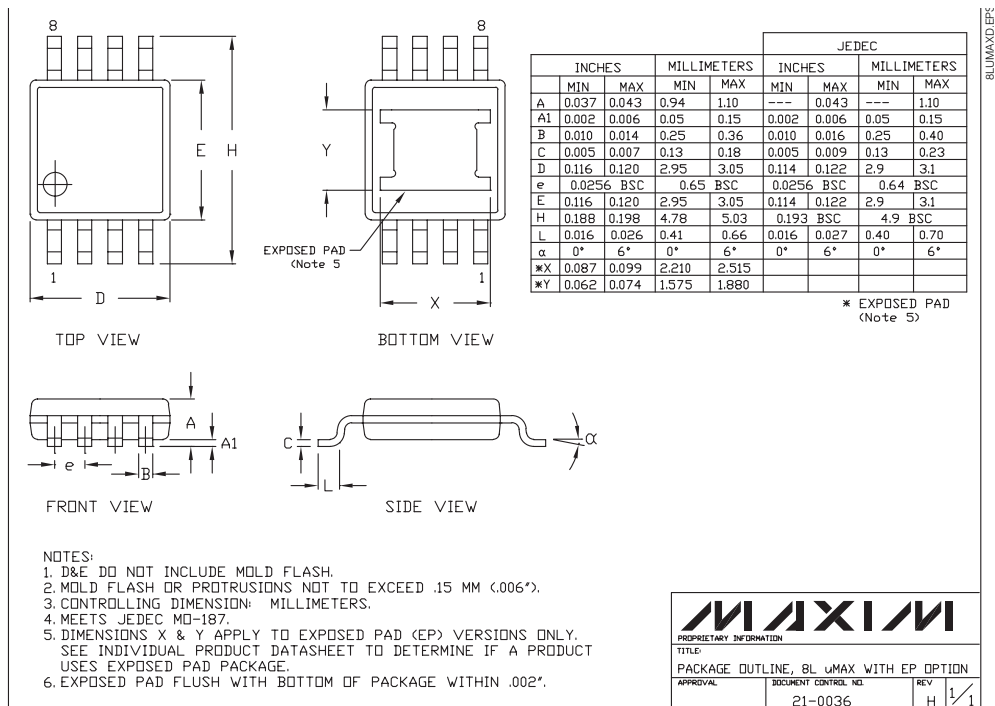


+3V/+5V, 250MHz, SOT23 ADC Buffer Amplifiers with High-Speed Disable

Package Information



6LSOT23



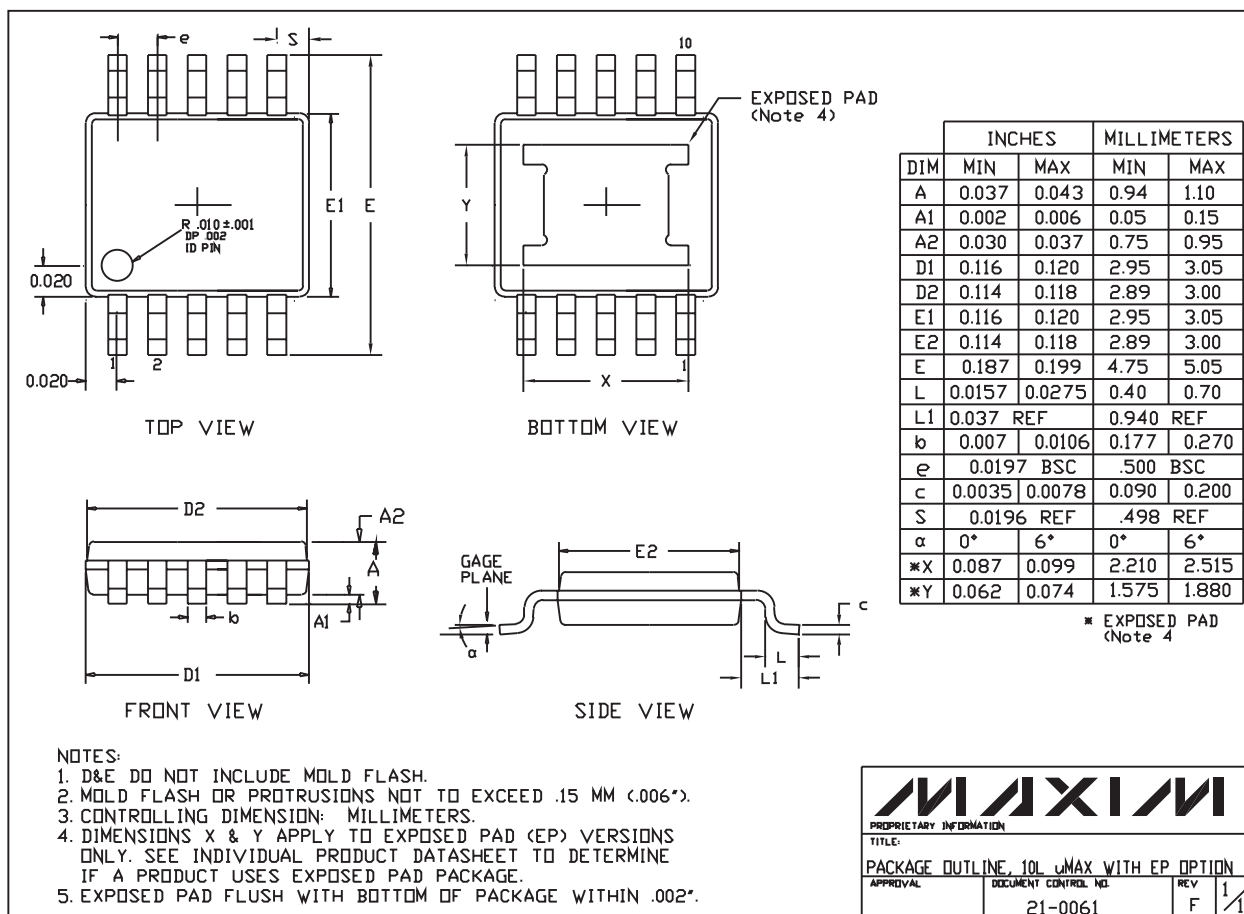
BLUMAXD BPS

+3V/+5V, 250MHz, SOT23 ADC Buffer Amplifiers with High-Speed Disable

Package Information (continued)

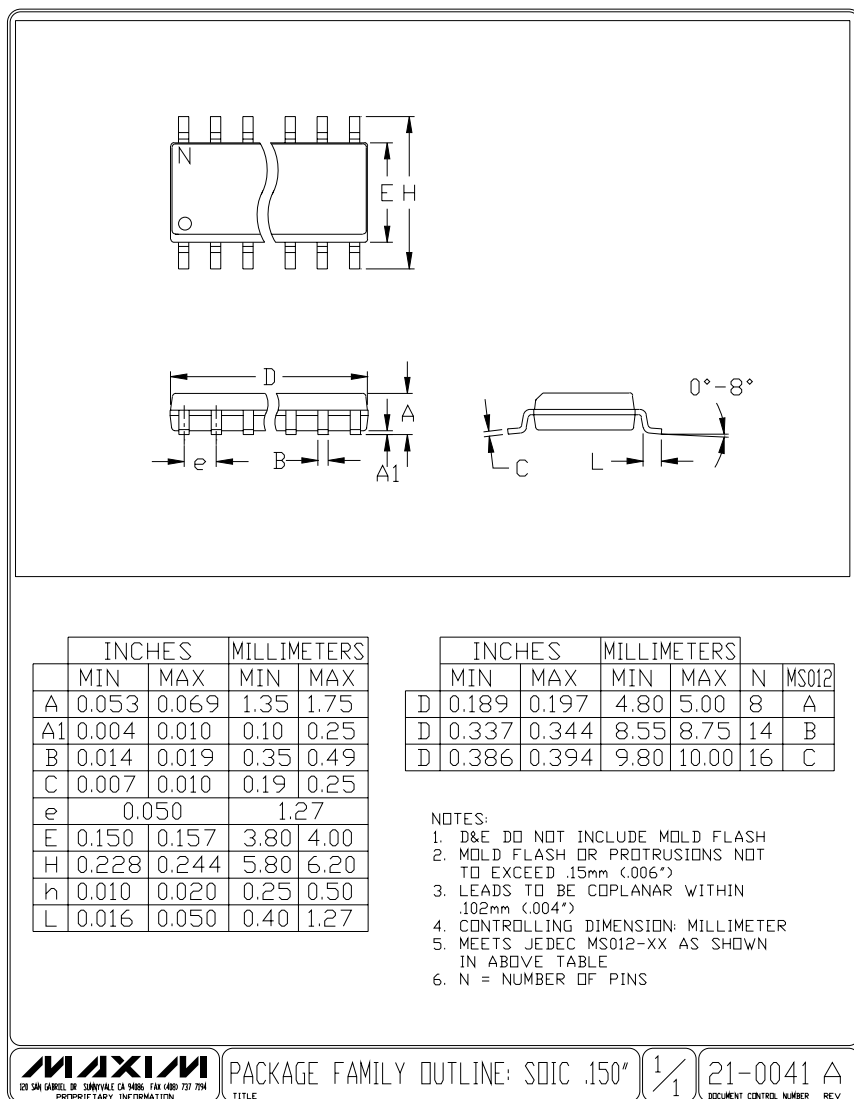
MAX4285-MAX4288/MAX4387/MAX4388

10LUMAX.EPS



+3V/+5V, 250MHz, SOT23 ADC Buffer Amplifiers with High-Speed Disable

Package Information (continued)



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