

# 74AHC2G241; 74AHCT2G241

Dual buffer/line driver; 3-state

Rev. 4 — 16 January 2019

Product data sheet

## 1. General description

The 74AHC2G241; 74AHCT2G241 is a high-speed Si-gate CMOS device.

The 74AHC2G241; 74AHCT2G241 is a dual non-inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs  $1\overline{OE}$  and 2OE. A HIGH level at pin  $1\overline{OE}$  causes output 1Y to assume a high-impedance OFF-state. A LOW level at pin 2OE causes output 2Y to assume a high-impedance OFF-state. Schmitt-trigger action at all inputs makes the circuit highly tolerant for slower input rise and fall times.

The AHC device has CMOS input switching levels and supply voltage range 2 V to 5.5 V.

The AHCT device has TTL input switching levels and supply voltage range 4.5 V to 5.5 V.

## 2. Features and benefits

- Symmetrical output impedance
- High noise immunity
- ESD protection:
  - HBM JESD22-A114E: exceeds 2000 V
  - MM JESD22-A115-A: exceeds 200 V
  - CDM JESD22-C101C: exceeds 1000 V
- Low power dissipation
- Balanced propagation delays
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

## 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHC2G241DP	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74AHC2G241DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74AHCT2G241DC				

## 4. Marking

Table 2. Marking

Type number	Marking code <sup>[1]</sup>
74AHC2G241DP	A241
74AHC2G241DC	A41
74AHCT2G241DC	C41

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

## 5. Functional diagram



Fig. 1. Logic symbol

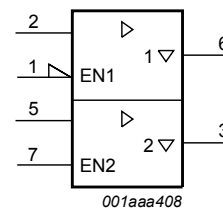


Fig. 2. IEC logic symbol

## 6. Pinning information

### 6.1. Pinning

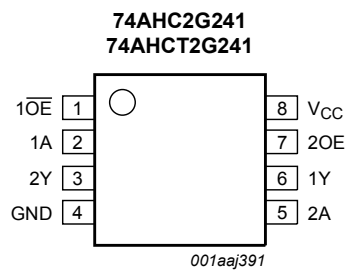


Fig. 3. Pin configuration SOT505-2 (TSSOP8) and SOT765-1 (VSSOP8)

## 6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
1OE	1	output enable input (active LOW)
1A	2	data input
2Y	3	data output
GND	4	ground (0 V)
2A	5	data input
1Y	6	data output
2OE	7	output enable input (active HIGH)
V <sub>CC</sub>	8	supply voltage

## 7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Input		Output	Input		Output
1OE	1A	1Y	2OE	2A	2Y
L	L	L	H	L	L
L	H	H	H	H	H
H	X	Z	L	X	Z

## 8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7.0	V
V <sub>I</sub>	input voltage		-0.5	+7.0	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V [1]	-20	-	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V [1]	-	±20	mA
I <sub>O</sub>	output current	-0.5 V < V <sub>O</sub> < V <sub>CC</sub> + 0.5 V	-	±25	mA
I <sub>CC</sub>	supply current		-	75	mA
I <sub>GND</sub>	ground current		-75	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C [2]	-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP8 package: above 55 °C the value of P<sub>tot</sub> derates linearly with 2.5 mW/K.

For VSSOP8 package: above 110 °C the value of P<sub>tot</sub> derates linearly with 8 mW/K.

## 9. Recommended operating conditions

**Table 6. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74AHC2G241			74AHCT2G241			Unit
			Min	Typ	Max	Min	Typ	Max	
V <sub>CC</sub>	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V <sub>I</sub>	input voltage		0	-	5.5	0	-	5.5	V
V <sub>O</sub>	output voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 3.3 V ± 0.3 V	-	-	100	-	-	-	ns/V
		V <sub>CC</sub> = 5.0 V ± 0.5 V	-	-	20	-	-	20	ns/V

## 10. Static characteristics

**Table 7. Static characteristics**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74AHC2G241</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V <sub>CC</sub> = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V <sub>CC</sub> = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V <sub>CC</sub> = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V <sub>CC</sub> = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	0.25	-	2.5	-	10	μA
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	1.0	-	10	-	40	μA
C <sub>I</sub>	input capacitance		-	1.5	10	-	10	-	10	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74AHCT2G241</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = -50 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -8.0 mA	3.94	-	-	3.8	-	3.70	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = 50 µA	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	0.25	-	2.5	-	10	µA
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	1.0	-	10	-	40	µA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>I</sub> = 3.4 V; other inputs at V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C <sub>I</sub>	input capacitance		-	1.5	10	-	10	-	10	pF

## 11. Dynamic characteristics

**Table 8. Dynamic characteristics**

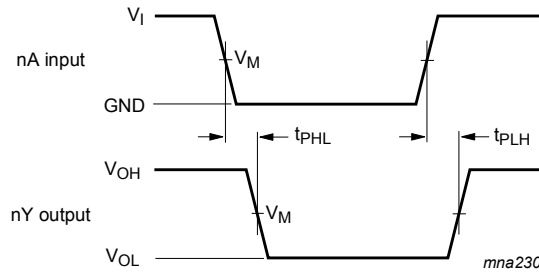
$GND = 0\text{ V}$ ; for test circuit see [Fig. 7](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74AHC2G241</b>										
$t_{pd}$	propagation delay	nA to nY; see <a href="#">Fig. 4</a> [1]								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ [2]								
		$C_L = 15\text{ pF}$	-	4.7	8.0	1.0	9.5	1.0	11.5	ns
		$C_L = 50\text{ pF}$	-	6.6	11.5	1.0	13.0	1.0	14.5	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ [3]								
		$C_L = 15\text{ pF}$	-	3.4	5.5	1.0	6.5	1.0	7.0	ns
$t_{en}$	enable time	$1\overline{OE}$ to 1Y; see <a href="#">Fig. 5</a> [1]								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ [2]								
		$C_L = 15\text{ pF}$	-	5.0	8.0	1.0	9.5	1.0	11.5	ns
		$C_L = 50\text{ pF}$	-	6.9	11.5	1.0	13.0	1.0	14.5	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ [3]								
		$C_L = 15\text{ pF}$	-	3.6	5.1	1.0	6.0	1.0	6.5	ns
		$C_L = 50\text{ pF}$	-	4.9	7.5	1.0	8.5	1.0	9.5	ns
		$2OE$ to 2Y; see <a href="#">Fig. 6</a> [1]								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ [2]								
		$C_L = 15\text{ pF}$	-	4.9	8.0	1.0	9.5	1.0	10.0	ns
		$C_L = 50\text{ pF}$	-	7.0	11.5	1.0	13.0	1.0	14.5	ns
		$t_{dis}$	disable time	$1\overline{OE}$ to 1Y; see <a href="#">Fig. 5</a> [1]						
$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ [2]										
$C_L = 15\text{ pF}$	-			6.0	9.7	1.0	11.5	1.0	12.5	ns
$C_L = 50\text{ pF}$	-			8.3	13.2	1.0	15.0	1.0	16.5	ns
$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ [3]										
$C_L = 15\text{ pF}$	-			4.1	6.8	1.0	8.0	1.0	8.5	ns
$C_L = 50\text{ pF}$	-			5.7	8.8	1.0	10.0	1.0	11.0	ns
$2OE$ to 2Y; see <a href="#">Fig. 6</a> [1]										
$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ [2]										
$C_L = 15\text{ pF}$	-			6.3	9.7	1.0	11.5	1.0	12.5	ns
$C_L = 50\text{ pF}$	-			9.0	13.2	1.0	15.0	1.0	16.5	ns
$C_{PD}$	power dissipation capacitance			per buffer; $C_L = 50\text{ pF}$ ; $f_i = 1\text{ MHz}$ ; $V_i = GND\text{ to }V_{CC}$ [4]	-	10	-	-	-	-

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74AHCT2G241</b>										
$t_{pd}$	propagation delay	nA to nY; see <a href="#">Fig. 4</a> [1]								
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ [3]								
		$C_L = 15 \text{ pF}$	-	3.4	5.5	1.0	6.5	1.0	7.0	ns
		$C_L = 50 \text{ pF}$	-	4.7	7.5	1.0	8.5	1.0	9.5	ns
$t_{en}$	enable time	$1\overline{OE}$ to 1Y; see <a href="#">Fig. 5</a> [1]								
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ [3]								
		$C_L = 15 \text{ pF}$	-	3.9	5.1	1.0	6.0	1.0	6.5	ns
		$C_L = 50 \text{ pF}$	-	5.1	7.5	1.0	8.5	1.0	9.5	ns
	$2OE$ to 2Y; see <a href="#">Fig. 6</a> [1]	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ [3]								
		$C_L = 15 \text{ pF}$	-	3.4	5.6	1.0	6.3	1.0	6.5	ns
		$C_L = 50 \text{ pF}$	-	4.8	7.5	1.0	9.0	1.0	9.5	ns
		disable time	$1\overline{OE}$ to 1Y; see <a href="#">Fig. 5</a> [1]							
$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ [3]										
$C_L = 15 \text{ pF}$	-		4.5	6.8	1.0	8.0	1.0	8.5	ns	
$C_L = 50 \text{ pF}$	-		6.1	8.8	1.0	10.0	1.0	11.0	ns	
$t_{dis}$	disable time	$2OE$ to 2Y; see <a href="#">Fig. 6</a> [1]								
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ [3]								
		$C_L = 15 \text{ pF}$	-	4.0	6.8	1.0	8.0	1.0	8.5	ns
		$C_L = 50 \text{ pF}$	-	5.7	8.8	1.0	10.0	1.0	11.0	ns
$C_{PD}$	power dissipation capacitance	per buffer; $C_L = 50 \text{ pF}$ ; $f_i = 1 \text{ MHz}$ ; $V_i = \text{GND to } V_{CC}$ [4]	-	10	-	-	-	-	-	pF

- [1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .  
 $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .  
 $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ .
- [2] Typical values are measured at  $V_{CC} = 3.3 \text{ V}$ .
- [3] Typical values are measured at  $V_{CC} = 5.0 \text{ V}$ .
- [4]  $C_{PD}$  is used to determine the dynamic power dissipation  $P_D$  ( $\mu\text{W}$ ).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  
 $f_o$  = output frequency in MHz;  
 $C_L$  = output load capacitance in pF;  
 $V_{CC}$  = supply voltage in Volts.

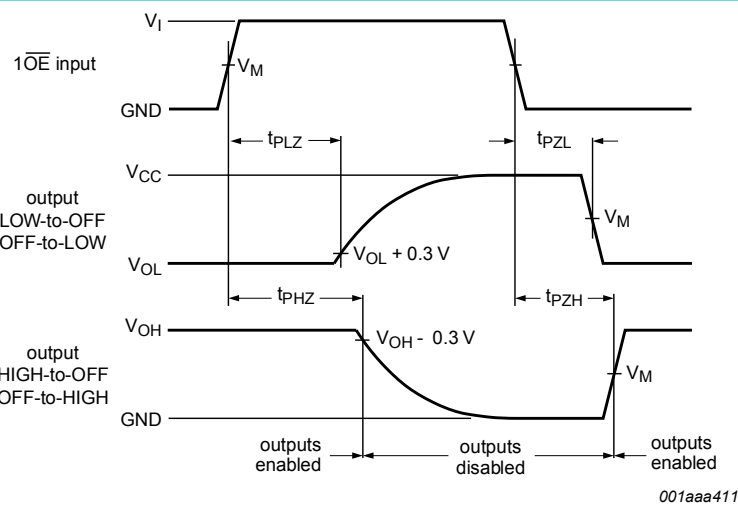
11.1. Waveforms and test circuit



Measurement points are given in [Table 9](#).

Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

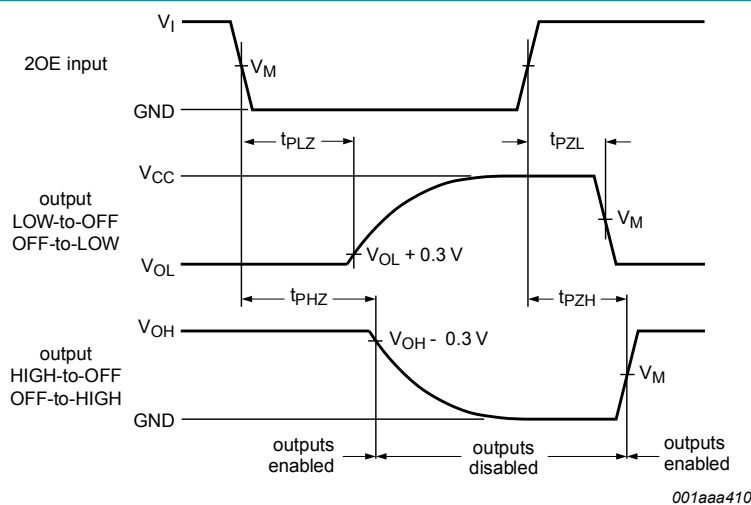
Fig. 4. The input (nA) to output (nY) propagation delays



Measurement points are given in [Table 9](#).

Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

Fig. 5. The input ( $\overline{1OE}$ ) to output 1Y enable and disable times



Measurement points are given in [Table 9](#).

Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

Fig. 6. The input (2OE) to output 2Y enable and disable times



Table 9. Measurement points

Type	Input	Output
	$V_M$	$V_M$
74AHC2G241	$0.5V_{CC}$	$0.5V_{CC}$
74AHCT2G241	1.5 V	$0.5V_{CC}$



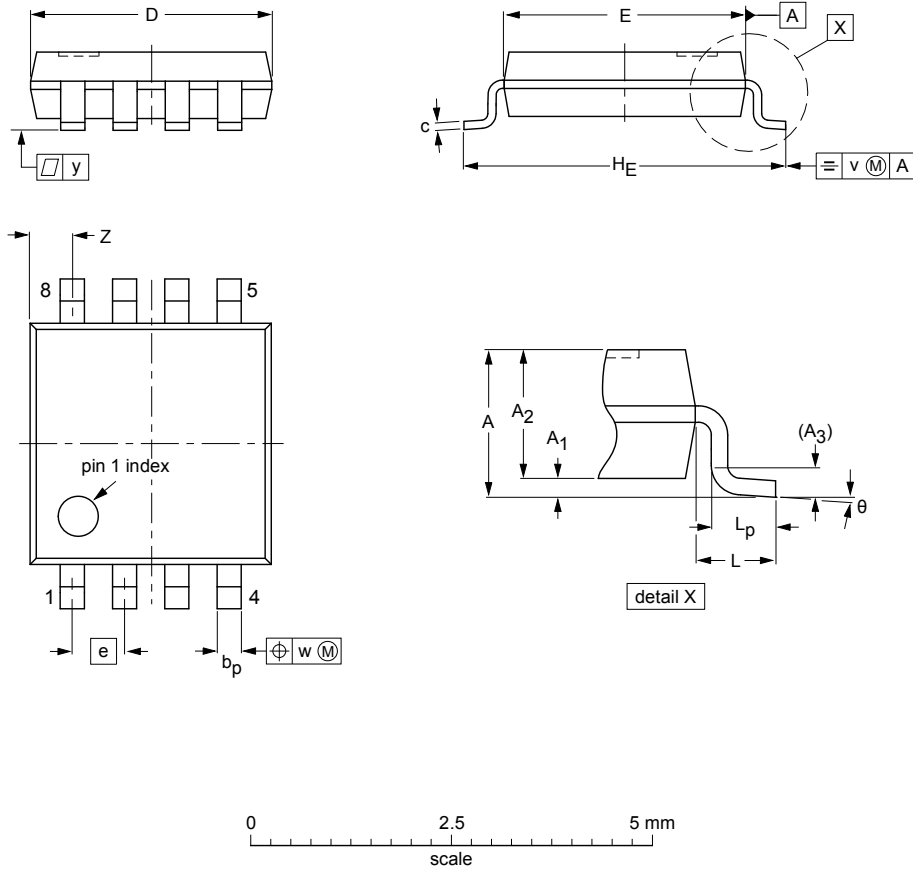
Fig. 7. Test circuit for measuring switching times

Table 10. Test data

Type	Input		Load		S1 position		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
74AHC2G241	$V_{CC}$	$\leq 3$ ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$
74AHCT2G241	3 V	$\leq 3$ ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$

12. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	v	w	y	Z <sup>(1)</sup>	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

Note

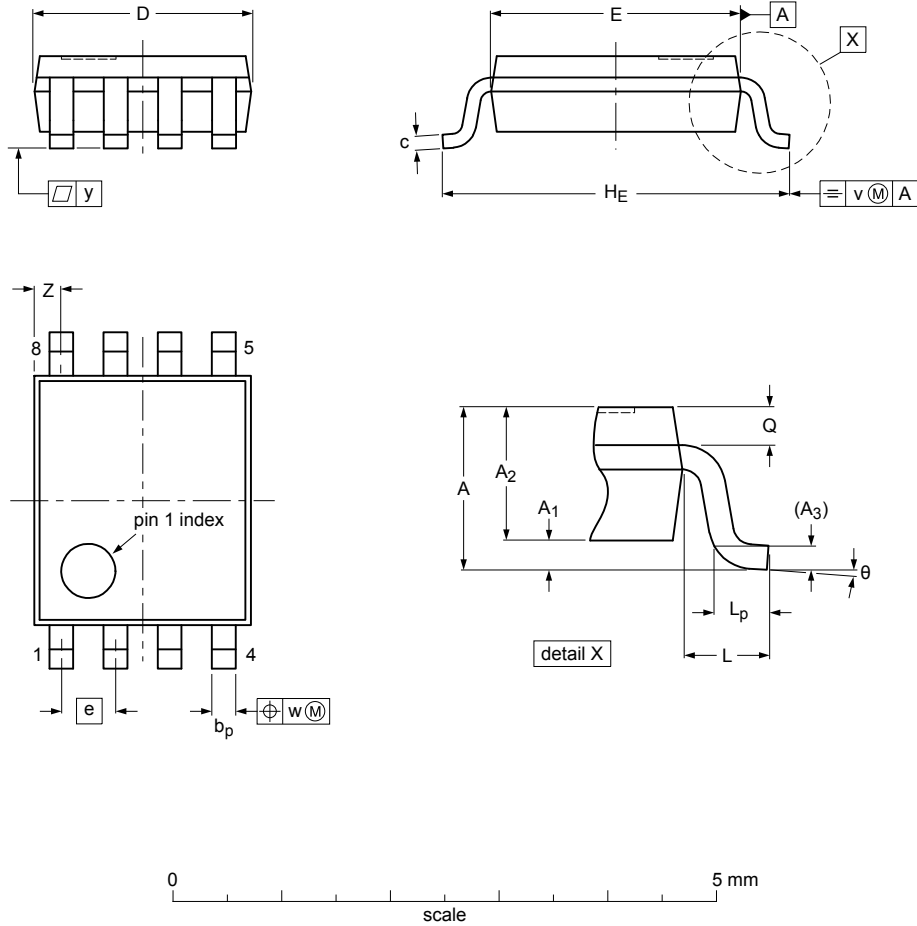
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		---				02-01-16

Fig. 8. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1



Dimensions (mm are the original dimensions)

Unit	A <sup>A</sup> max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
max		0.15	0.85		0.27	0.23	2.1	2.4		3.2		0.40	0.21				0.4	8°
mm	nom	1		0.12					0.5		0.4			0.2	0.08	0.1		
	min		0.00	0.60	0.17	0.08	1.9	2.2		3.0		0.15	0.19				0.1	0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

sot765-1\_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT765-1		MO-187			07-06-02-16-05-31

Fig. 9. Package outline SOT765-1 (VSSOP8)

## 13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT2G241 v.4	20190116	Product data sheet	-	74AHC_AHCT2G241 v.3
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Type numbers 74AHCT2G241DP, 74AHC2G241GD and 74AHCT2G241GD removed.</li> </ul>			
74AHC_AHCT2G241 v.3	20130513	Product data sheet	-	74AHC_AHCT2G241 v.2
Modifications:	<ul style="list-style-type: none"> <li>For type number 74AHC2G241GD and 74AHCT2G241GD XSON8U has changed to XSON8.</li> </ul>			
74AHC_AHCT2G241 v.2	20090113	Product data sheet	-	74AHC_AHCT2G241 v.1
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Added type number 74AHC2G241GD and 74AHCT2G241GD (XSON8U package).</li> </ul>			
74AHC_AHCT2G241 v.1	20040310	Product data	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
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