

Programmable Timing Control Hub™ for Next Gen P4™ processor

Recommended Application:

CK410 compliant clock

Output Features:

- 2 - 0.7V current-mode differential CPU pairs
- 1 - 0.7V current-mode differential SRC pair
- 6 - PCI (33MHz)
- 3 - PCICLK_F, (33MHz) free-running
- 1 - USB, 48MHz
- 1 - 24/48 MHz
- 1 - DOT, 96MHz, 0.7V current differential pair
- 2 - REF, 14.318MHz
- 5 - PCI-Express 0.7V current differential pairs

Key Specifications:

- CPU/SRC outputs cycle-cycle jitter < 85ps
- PCI outputs cycle-cycle jitter < 250ps
- +/- 300ppm frequency accuracy on CPU & SRC clocks

Functionality

Bit4	Bit3	Bit2 FSLC	Bit1 FSLB	Bit0 FSLA	CPU MHz	PCIEX MHz	SRC MHz	PCI MHz
0	0	0	0	0	266.66	100.00	100.00	33.33
0	0	0	0	1	133.33	100.00	100.00	33.33
0	0	0	1	0	200.00	100.00	100.00	33.33
0	0	0	1	1	166.66	100.00	100.00	33.33
0	0	1	0	0	333.33	100.00	100.00	33.33
0	0	1	0	1	100.00	100.00	100.00	33.33
0	0	1	1	0	400.00	100.00	100.00	33.33
0	0	1	1	1	200.00	100.00	100.00	33.33
0	1	0	0	0	266.66	133.33	133.33	33.33
0	1	0	0	1	133.33	133.33	133.33	33.33
0	1	0	1	0	200.00	133.33	133.33	33.33
0	1	0	1	1	166.66	125.00	125.00	33.33
0	1	1	0	0	333.33	125.00	125.00	33.33
0	1	1	0	1	100.00	133.33	133.33	33.33
0	1	1	1	0	400.00	133.33	133.33	33.33
0	1	1	1	1	200.00	133.33	133.33	33.33
1	0	0	0	0	269.33	101.00	101.00	33.67
1	0	0	0	1	134.66	101.00	101.00	33.67
1	0	0	1	0	202.00	101.00	101.00	33.67
1	0	0	1	1	168.33	101.00	101.00	33.67
1	0	1	0	0	274.66	103.00	103.00	34.33
1	0	1	0	1	137.33	103.00	103.00	34.33
1	0	1	1	0	206.00	103.00	103.00	34.33
1	0	1	1	1	171.66	103.00	103.00	34.33
1	1	0	0	0	279.99	105.00	105.00	35.00
1	1	0	0	1	140.00	105.00	105.00	35.00
1	1	0	1	0	210.00	105.00	105.00	35.00
1	1	0	1	1	174.99	105.00	105.00	35.00
1	1	1	0	0	287.99	108.00	108.00	36.00
1	1	1	0	1	144.00	108.00	108.00	36.00
1	1	1	1	0	216.00	108.00	108.00	36.00
1	1	1	1	1	179.99	108.00	108.00	36.00

* Entries 00111 & 01111 are 250MHz on the B & C revision.

Features/Benefits:

- Programmable output frequencies
- Programmable output skew.
- Programmable spread percentage for EMI control.
- Programmable watch dog safe frequency.
- Supports tight ppm accuracy clocks for Serial-ATA
- Supports spread spectrum modulation, 0 to -0.5% down spread, ±0.25% center spread, and ±0.3% center spread
- Uses external 14.318MHz crystal, external crystal load caps are required for frequency tuning
- Supports undriven differential CPU, SRC pair in PD# for power management.

Pin Configuration

GND	1	56	VDDPCI
PCICLK3	2	55	PCICLK2
PCICLK4	3	54	PCICLK1
PCICLK5	4	53	PCICLK0
GND	5	52	Reset#
VDDPCI	6	51	REF0/FS _L C
PCICLK_F0	7	50	REF1
FS _L A/PCICLK_F1	8	49	GND
FS _L B/PCICLK_F2	9	48	X1
VDD48	10	47	X2
**SEL24_48#/24_48MHz	11	46	VDDREF
USB_48MHz	12	45	SCLK
GND	13	44	SDATA
DOTT_96MHz	14	43	CPUCLKT0
DOTC_96MHz	15	42	CPUCLKC0
Vtt_PwrGd#/PD	16	41	VDDCPU
PCIEXT0	17	40	CPUCLKT1
PCIEXC0	18	39	CPUCLKC1
VDDPCIEX	19	38	GND
GND	20	37	IREF
PCIEXT1	21	36	GNDA
PCIEXC1	22	35	VDDA
PCIEXT2	23	34	VDDPCIEX
PCIEXC2	24	33	PCIEXT4
GND	25	32	PCIEXC4
SRCCLKT	26	31	PCIEXT3
SRCCLKC	27	30	PCIEXC3
VDDSRC	28	29	GND

ICS954119

56-Pin SSOP

* Internal Pull-Up Resistor

** Internal Pull-Down Resistor

Pin Description

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	GND	PWR	Ground pin.
2	PCICLK3	OUT	PCI clock output.
3	PCICLK4	OUT	PCI clock output.
4	PCICLK5	OUT	PCI clock output.
5	GND	PWR	Ground pin.
6	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
7	PCICLK_F0	OUT	Free running PCI clock not affected by PCI_STOP# .
8	FSLA/PCICLK_F1	I/O	3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. / 3.3V PCI free running clock output.
9	FSLB/PCICLK_F2	I/O	3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values./ 3.3V PCI free running clock output.
10	VDD48	PWR	Power pin for the 48MHz output.3.3V
11	**SEL24_48#/24_48MHz	I/O	Latched select input for 24/48MHz output / 24/48MHz clock output. 1=24MHz, 0 = 48MHz.
12	USB_48MHz	OUT	48.00MHz USB clock
13	GND	PWR	Ground pin.
14	DOTT_96MHz	OUT	True clock of differential pair for 96.00MHz DOT clock.
15	DOTC_96MHz	OUT	Complement clock of differential pair for 96.00MHz DOT clock.
16	Vtt_PwrGd#/PD	IN	Vtt_PwrGd# is an active low input used to determine when latched inputs are ready to be sampled. PD is an asynchronous active high input pin used to put the device into a low power state. The internal clocks, PLLs and the crystal oscillator are stopped.
17	PCIEXT0	OUT	True clock of differential PCI_Express pair.
18	PCIEXC0	OUT	Complement clock of differential PCI_Express pair.
19	VDDPCIEX	PWR	Power supply for PCI Express clocks, nominal 3.3V
20	GND	PWR	Ground pin.
21	PCIEXT1	OUT	True clock of differential PCI_Express pair.
22	PCIEXC1	OUT	Complement clock of differential PCI_Express pair.
23	PCIEXT2	OUT	True clock of differential PCI_Express pair.
24	PCIEXC2	OUT	Complement clock of differential PCI_Express pair.
25	GND	PWR	Ground pin.
26	SRCCLKT	OUT	True clock of differential pair for S-ATA support. +/- 300ppm accuracy required.
27	SRCCLKC	OUT	Complement clock of differential pair for S-ATA support. +/- 300ppm accuracy required.
28	VDDSRC	PWR	Supply for SRC clocks, 3.3V nominal

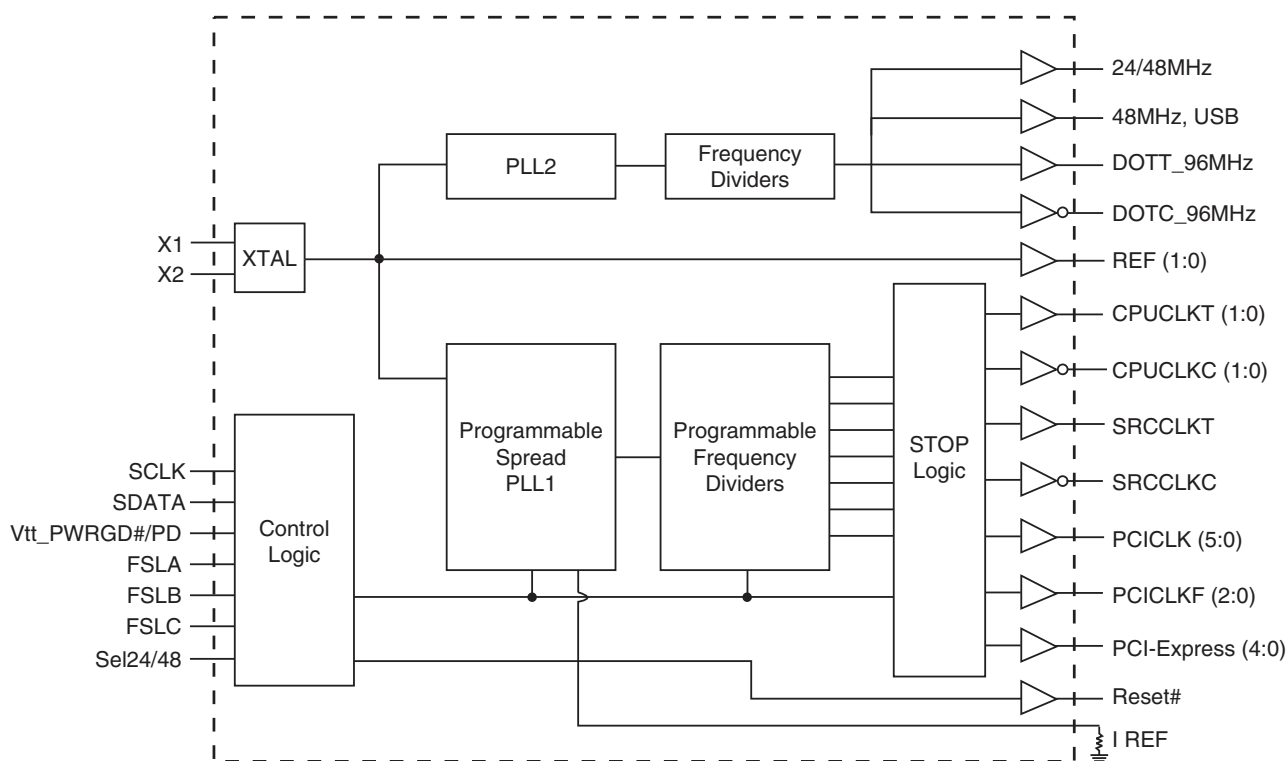
Pin Description

PIN #	PIN NAME	TYPE	DESCRIPTION
29	GND	PWR	Ground pin.
30	PCIEXC3	OUT	Complement clock of differential PCI_Express pair.
31	PCIEXT3	OUT	True clock of differential PCI_Express pair.
32	PCIEXC4	OUT	Complement clock of differential PCI_Express pair.
33	PCIEXT4	OUT	True clock of differential PCI_Express pair.
34	VDDPCIEX	PWR	Power supply for PCI Express clocks, nominal 3.3V
35	VDDA	PWR	3.3V power for the PLL core.
36	GNDA	PWR	Ground pin for the PLL core.
37	IREF	OUT	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.
38	GND	PWR	Ground pin.
39	CPUCLKC1	OUT	Complimentary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
40	CPUCLKT1	OUT	True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
41	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
42	CPUCLKC0	OUT	Complimentary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
43	CPUCLKT0	OUT	True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
44	SDATA	I/O	Data pin for SMBus circuitry, 5V tolerant.
45	SCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.
46	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
47	X2	OUT	Crystal output, Nominally 14.318MHz
48	X1	IN	Crystal input, Nominally 14.318MHz.
49	GND	PWR	Ground pin.
50	REF1	OUT	14.318 MHz reference clock.
51	REF0/FSLC	I/O	14.318 MHz reference clock./ 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values.
52	Reset#	OUT	Real time system reset signal for frequency gear ratio change or watchdog timer timeout. This signal is active low.
53	PCICLK0	OUT	PCI clock output.
54	PCICLK1	OUT	PCI clock output.
55	PCICLK2	OUT	PCI clock output.
56	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V

General Description

ICS954119 follows Intel CK410 Yellow Cover specification. This clock synthesizer provides a single chip solution for next generation P4 Intel processors and Intel chipsets. **ICS954119** is driven with a 14.318MHz crystal.

Block Diagram



Power Busing

VDD	GND	Description
6,56	1,5	PCI pads and Prepad
10	13	USB_48MHz, DOT_96MHz, Fix PLL
19,34	20,29	Differential PCIEX pair
28	25	Differential SRC pair
35	36	Analog Core, CPU PLL
41	38	Differential CPU pair
46	49	Xtal, Ref, CPU PLL Digital

General I²C serial interface information for the ICS954119

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2_(H)
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) sends the data byte count = X
- ICS clock will **acknowledge**
- Controller (host) starts sending **Byte N through Byte N + X - 1**
(see Note 2)
- ICS clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

Index Block Write Operation		
Controller (Host)		ICS (Slave/Receiver)
T	starT bit	
Slave Address D2 _(H)		
WR	WRite	
		ACK
Beginning Byte = N		
		ACK
Data Byte Count = X		
		ACK
Beginning Byte N		
		ACK
○		
○		
○		
Byte N + X - 1		
		ACK
P	stoP bit	

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2_(H)
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3_(H)
- ICS clock will **acknowledge**
- ICS clock will send the data byte count = X
- ICS clock sends **Byte N + X - 1**
- ICS clock sends **Byte 0 through byte X (if X_(H) was written to byte 8).**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation		
Controller (Host)		ICS (Slave/Receiver)
T	starT bit	
Slave Address D2 _(H)		
WR	WRite	
		ACK
Beginning Byte = N		
		ACK
RT	Repeat starT	
Slave Address D3 _(H)		
RD	ReaD	
		ACK
		Data Byte Count = X
ACK		
ACK		
○		
○		
○		
		Byte N + X - 1
N	Not acknowledge	
P	stoP bit	

Table1: Frequency Selection Table

Bit4	Bit3	Bit2	Bit1	Bit0	CPU	PCIEX	SRC	PCI	Spread
		FSLC	FSLB	FSLA	MHz	MHz	MHz	MHz	%
0	0	0	0	0	266.66	100.00	100.00	33.33	0 to -0.5% Down
0	0	0	0	1	133.33	100.00	100.00	33.33	0 to -0.5% Down
0	0	0	1	0	200.00	100.00	100.00	33.33	0 to -0.5% Down
0	0	0	1	1	166.66	100.00	100.00	33.33	0 to -0.5% Down
0	0	1	0	0	333.33	100.00	100.00	33.33	0 to -0.5% Down
0	0	1	0	1	100.00	100.00	100.00	33.33	0 to -0.5% Down
0	0	1	1	0	400.00	100.00	100.00	33.33	0 to -0.5% Down
0	0	1	1	1	200.00	100.00	100.00	33.33	0 to -0.5% Down
0	1	0	0	0	266.66	133.33	133.33	33.33	+/-0.25% Center
0	1	0	0	1	133.33	133.33	133.33	33.33	+/-0.25% Center
0	1	0	1	0	200.00	133.33	133.33	33.33	+/-0.25% Center
0	1	0	1	1	166.66	125.00	125.00	33.33	+/-0.25% Center
0	1	1	0	0	333.33	125.00	125.00	33.33	+/-0.25% Center
0	1	1	0	1	100.00	133.33	133.33	33.33	+/-0.25% Center
0	1	1	1	0	400.00	133.33	133.33	33.33	+/-0.25% Center
0	1	1	1	1	200.00	133.33	133.33	33.33	+/-0.25% Center
1	0	0	0	0	269.33	101.00	101.00	33.67	+/-0.3% Center
1	0	0	0	1	134.66	101.00	101.00	33.67	+/-0.3% Center
1	0	0	1	0	202.00	101.00	101.00	33.67	+/-0.3% Center
1	0	0	1	1	168.33	101.00	101.00	33.67	+/-0.3% Center
1	0	1	0	0	274.66	103.00	103.00	34.33	+/-0.3% Center
1	0	1	0	1	137.33	103.00	103.00	34.33	+/-0.3% Center
1	0	1	1	0	206.00	103.00	103.00	34.33	+/-0.3% Center
1	0	1	1	1	171.66	103.00	103.00	34.33	+/-0.3% Center
1	1	0	0	0	279.99	105.00	105.00	35.00	+/-0.3% Center
1	1	0	0	1	140.00	105.00	105.00	35.00	+/-0.3% Center
1	1	0	1	0	210.00	105.00	105.00	35.00	+/-0.3% Center
1	1	0	1	1	174.99	105.00	105.00	35.00	+/-0.3% Center
1	1	1	0	0	287.99	108.00	108.00	36.00	+/-0.3% Center
1	1	1	0	1	144.00	108.00	108.00	36.00	+/-0.3% Center
1	1	1	1	0	216.00	108.00	108.00	36.00	+/-0.3% Center
1	1	1	1	1	179.99	108.00	108.00	36.00	+/-0.3% Center

IC Table: Frequency Select Register

Byte 0	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	FS Source	Frequency H/W IIC Select	RW	Latch Inputs	IIC	0
Bit 6	-	SS_EN1	PLL1 Spread Enable	RW	OFF	ON	1
Bit 5	-	Reserved	Reserved	RW	-	-	1
Bit 4	-	Bit4	Freq Select Bit 4	RW	See Table 1: PLL 1 Frequency Selection Table		0
Bit 3	-	Bit3	Freq Select Bit 3	RW			0
Bit 2	-	FSLC	Freq Select Bit 2	RW			Latch
Bit 1	-	FSLB	Freq Select Bit 1	RW			Latch
Bit 0	-	FSLA	Freq Select Bit 0	RW			Latch

IC Table: Output Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	7	PCICLK_F0	Output Control	RW	Disable	Enable	1
Bit 6	14,15	DOTT/C_96MHz	Output Control	RW	Disable	Enable	1
Bit 5	12	USB_48MHz	Output Control	RW	Disable	Enable	1
Bit 4	51	REF0	Output Control	RW	Disable	Enable	1
Bit 3	50	REF1	Output Control	RW	Disable	Enable	1
Bit 2	40,39	CPUCLKT/C1	Output Control	RW	Disable	Enable	1
Bit 1	43,42	CPUCLKT/C0	Output Control	RW	Disable	Enable	1
Bit 0	-	CPUCLK's	PD Mode Output State Control	RW	Driven	Hi-Z	0

IC Table: Output Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	4	PCICLK5	Output Control	RW	Disable	Enable	1
Bit 6	3	PCICLK4	Output Control	RW	Disable	Enable	1
Bit 5	2	PCICLK3	Output Control	RW	Disable	Enable	1
Bit 4	55	PCICLK2	Output Control	RW	Disable	Enable	1
Bit 3	54	PCICLK1	Output Control	RW	Disable	Enable	1
Bit 2	53	PCICLK0	Output Control	RW	Disable	Enable	1
Bit 1	9	PCICLK_F2	Output Control	RW	Disable	Enable	1
Bit 0	8	PCICLK_F1	Output Control	RW	Disable	Enable	1

IC Table: Output Control Register

Byte 3	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	PCIEXCLK's	PD Mode Output State Control	RW	Driven	Hi-Z	0
Bit 6	-	Reserved	Reserved	RW	-	-	1
Bit 5	33,32	PCIEXCLKT/C4	Output Control	RW	Disable	Enable	1
Bit 4	31,30	PCIEXCLKT/C3	Output Control	RW	Disable	Enable	1
Bit 3	27,26	SRCCLKT/C	Output Control	RW	Disable	Enable	1
Bit 2	24,23	PCIEXCLKT/C2	Output Control	RW	Disable	Enable	1
Bit 1	22,21	PCIEXCLKT/C1	Output Control	RW	Disable	Enable	1
Bit 0	18,17	PCIEXCLKT/C0	Output Control	RW	Disable	Enable	1

IC Table: Output Control Register

Byte 4	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	PCI/SRC Stop EN	Stop all PCI / PCIe / SRC clocks		Enable	Disable	1
Bit 6	-	PCICLK_F2	Stop Control	RW	Free Running	Stoppable	0
Bit 5	-	PCICLK_F1	Stop Control	RW	Free Running	Stoppable	0
Bit 4	-	PCICLK_F0	Stop Control	RW	Free Running	Stoppable	0
Bit 3	-	PCIEXCLKT/C (5:3)	Stop Control	RW	Free Running	Stoppable	1
Bit 2	-	SRCCLKT/C	Stop Control	RW	Free Running	Stoppable	1
Bit 1	-	PCIEXCLKT/C (2:0)	Stop Control	RW	Free Running	Stoppable	1
Bit 0	-	Reserved	Reserved	RW	-	-	1

PC Table: Programmable Skew Control Register

Byte 5	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	PCISkw3	CPU-PCI 7 Steps Skew Control (ps)	RW	0000:0	0100:150	0
Bit 6	-	PCISkw2		RW	0001:N/A	0101:N/A	0
Bit 5	-	PCISkw1		RW	0010:N/A	0110:N/A	0
Bit 4	-	PCISkw0		RW	0011:N/A	0111:N/A	0
Bit 3	-	ASYNC1	PCI Async Freq	RW	00 = PLL1	10 = 37.7	0
Bit 2	-	ASYNC0		RW	01 = 33.0	11 = 44.0	0
Bit 1	-	REF0	REF0 select	RW	XTAL	Fixed PLL	0
Bit 0	-	Reserved	Reserved	RW	-	-	0

PC Table: Output Drive Control Register

Byte 6	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	1
Bit 6	-	Reserved		RW	-	-	1
Bit 5	-	Reserved	Reserved	RW	-	-	1
Bit 4	-	Reserved		RW	-	-	1
Bit 3	-	Reserved	Reserved	RW	-	-	0
Bit 2	-	Reserved		RW	-	-	1
Bit 1	-	Reserved	Reserved	RW	-	-	0
Bit 0	-	Reserved		RW	-	-	1

PC Table: Vendor ID Register

Byte 7	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	0
Bit 6	-	Reserved	Reserved	RW	-	-	0
Bit 5	-	Reserved	Reserved	RW	-	-	0
Bit 4	-	Reserved	Reserved	RW	-	-	0
Bit 3	-	VID3	VENDOR ID	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	001 = ICS	-	0
Bit 0	-	VID0		R	-	-	1

PC Table: Byte Count Register

Byte 8	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	BC7	Byte Count Programming b(7:0)	RW	Writing to this register will configure how many bytes will be read back, default is 0F = 15 bytes.		0
Bit 6	-	BC6		RW			0
Bit 5	-	BC5		RW			0
Bit 4	-	BC4		RW			0
Bit 3	-	BC3		RW			1
Bit 2	-	BC2		RW			1
Bit 1	-	BC1		RW			1
Bit 0	-	BC0		RW			1

PC Table: WD Time Control Register

Byte 9	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	WD_EN	Watchdog Alarm Enable	RW	Disable	Enable	0
Bit 6	-	WD_SEL	Watchdog Hard/Soft Alarm Select	RW	Hard only	Hard and Soft	0
Bit 5	-	WD Hard Status	WD Hard Alarm Status	R	Normal	Alarm	X
Bit 4	-	WD Soft Status	WD Soft Alarm Status	R	Normal	Alarm	X
Bit 3	-	WDTCtrl	Watch Dog Time base Control	RW	290ms Base	1160ms Base	0
Bit 2	-	WD2	WD Timer Bit 2	RW	These bits represent X*290ms (or 1.16S) the watchdog timer waits before it goes to alarm mode. Default is 7 X 290ms = 2s.		1
Bit 1	-	WD1	WD Timer Bit 1	RW			1
Bit 0	-	WD0	WD Timer Bit 0	RW			1

IC Table: M/N Programming & WD Safe Frequency Control Register

Byte 10	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	M/N_EN	PLL1 M/N Programming Enable	RW	Disable	Enable	0
Bit 6	-	Reserved	Reserved	RW	-	-	0
Bit 5	-	WD Safe Freq Source	WD Safe Freq Source	RW	B10b(4:0)	Latch Inputs	0
Bit 4	-	WD SF4	Watch Dog Safe Freq Programming bits	RW	Writing to these bit will configure the safe frequency as Byte0 bit (4:0).		0
Bit 3	-	WD SF3		RW			0
Bit 2	-	WD SF2		RW			0
Bit 1	-	WD SF1		RW			0
Bit 0	-	WD SF0		RW			0

IC Table: PLL1 Frequency Control Register

Byte 11	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div8	N Divider Prog bit 8	RW	The decimal representation of M and N Divider in Byte 11 and 12 will configure the PLL1 VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	N Div9	N Divider Prog bit 9	RW			X
Bit 5	-	M Div5	M Divider Programming bit (5:0)	RW			X
Bit 4	-	M Div4		RW			X
Bit 3	-	M Div3		RW			X
Bit 2	-	M Div2		RW			X
Bit 1	-	M Div1		RW			X
Bit 0	-	M Div0		RW			X

IC Table: PLL1 Frequency Control Register

Byte 12	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div7	N Divider Programming Byte12 bit(7:0) and Byte11 bit(7:6)	RW	The decimal representation of M and N Divider in Byte 11 and 12 will configure the PLL1 VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	N Div6		RW			X
Bit 5	-	N Div5		RW			X
Bit 4	-	N Div4		RW			X
Bit 3	-	N Div3		RW			X
Bit 2	-	N Div2		RW			X
Bit 1	-	N Div1		RW			X
Bit 0	-	N Div0		RW			X

IC Table: PLL1 Spread Spectrum Control Register

Byte 13	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SSP7	Spread Spectrum Programming bit(7:0)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread percentage of PLL1		X
Bit 6	-	SSP6		RW			X
Bit 5	-	SSP5		RW			X
Bit 4	-	SSP4		RW			X
Bit 3	-	SSP3		RW			X
Bit 2	-	SSP2		RW			X
Bit 1	-	SSP1		RW			X
Bit 0	-	SSP0		RW			X

IC Table: PLL1 Spread Spectrum Control Register

Byte 14	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	R	-	-	0
Bit 6	-	SSP14	Spread Spectrum Programming bit(14:8)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread percentage of PLL1		X
Bit 5	-	SSP13		RW			X
Bit 4	-	SSP12		RW			X
Bit 3	-	SSP11		RW			X
Bit 2	-	SSP10		RW			X
Bit 1	-	SSP9		RW			X
Bit 0	-	SSP8		RW			X

IC Table: Reserved Register

Byte 15	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	Reserved		X
Bit 6	-	Reserved	Reserved	RW			X
Bit 5	-	Reserved	Reserved	RW			X
Bit 4	-	Reserved	Reserved	RW			X
Bit 3	-	Reserved	Reserved	RW			X
Bit 2	-	Reserved	Reserved	RW			X
Bit 1	-	Reserved	Reserved	RW			X
Bit 0	-	Reserved	Reserved	RW			X

IC Table: Reserved Register

Byte 16	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	Reserved		X
Bit 6	-	Reserved		RW			X
Bit 5	-	Reserved		RW			X
Bit 4	-	Reserved		RW			X
Bit 3	-	Reserved		RW			X
Bit 2	-	Reserved		RW			X
Bit 1	-	Reserved		RW			X
Bit 0	-	Reserved		RW			X

IC Table: Reserved Register

Byte 17	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	Reserved		X
Bit 6	-	Reserved		RW			X
Bit 5	-	Reserved		RW			X
Bit 4	-	Reserved		RW			X
Bit 3	-	Reserved		RW			X
Bit 2	-	Reserved		RW			X
Bit 1	-	Reserved		RW			X
Bit 0	-	Reserved		RW			X

IC Table: Reserved Register

Byte 18	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	Reserved		0
Bit 6	-	Reserved		RW			X
Bit 5	-	Reserved		RW			X
Bit 4	-	Reserved		RW			X
Bit 3	-	Reserved		RW			X
Bit 2	-	Reserved		RW			X
Bit 1	-	Reserved		RW			X
Bit 0	-	Reserved		RW			X

IC Table: Programmable Output Divider Register

Byte 19		Pin #	Name	Control Function	Type	0		1		PWD
Bit 7	-		CPUDiv3	CPU Divider Ratio Programming Bits	RW	0000:/2	0100:/4	1000:/8	1100:/16	X
Bit 6	-		CPUDiv2		RW	0001:/3	0101:/6	1001:/12	1101:/24	X
Bit 5	-		CPUDiv1		RW	0010:/5	0110:/10	1010:/20	1110:/40	X
Bit 4	-		CPUDiv0		RW	0011:/7	0111:/14	1011:/28	1111:/56	X
Bit 3	-		PCIEXDiv3	PCIEX Divider Ratio Programming Bits	RW	0000:/2	0100:/4	1000:/8	1100:/16	X
Bit 2	-		PCIEXDiv2		RW	0001:/3	0101:/6	1001:/12	1101:/24	X
Bit 1	-		PCIEXDiv1		RW	0010:/5	0110:/10	1010:/20	1110:/40	X
Bit 0	-		PCIEXDiv0		RW	0011:/7	0111:/14	1011:/28	1111:/56	X

I²C Table: Programmable Output Divider Register

Byte 20	Pin #	Name	Control Function	Type	0		1		PWD
Bit 7	-	PCIDiv3	PCI Divider Ratio Programming Bits	RW	0000:/2	0100:/4	1000:/8	1100:/16	X
Bit 6	-	PCIDiv2		RW	0001:/3	0101:/6	1001:/12	1101:/24	X
Bit 5	-	PCIDiv1		RW	0010:/5	0110:/10	1010:/20	1110:/40	X
Bit 4	-	PCIDiv0		RW	0011:/15	0111:/30	1011:/60	1111:/120	X
Bit 3	-	Reserved	Reserved	RW	-	-	-	-	X
Bit 2	-	Reserved		RW	-	-	-	-	X
Bit 1	-	Reserved		RW	-	-	-	-	X
Bit 0	-	Reserved		RW	-	-	-	-	X

Absolute Maximum Rating

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
3.3V Core Supply Voltage	VDD_A	-			V _{DD} + 0.5V	V	1
3.3V Logic Input Supply Voltage	VDD_In	-	GND - 0.5		V _{DD} + 0.5V	V	1
Storage Temperature	Ts	-	-65		150	°C	1
Ambient Operating Temp	Tambient	-	0		70	°C	1
Case Temperature	Tcase	-			115	°C	1
Input ESD protection HBM	ESD prot	-	2000			V	1

¹Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	Notes
Input High Voltage	V _{IH}	3.3 V +/-5%	2		V _{DD} + 0.3	V	1
Input Low Voltage	V _{IL}	3.3 V +/-5%	V _{SS} - 0.3		0.8	V	1
Input High Current	I _{IH}	V _{IN} = V _{DD}	-5		5	uA	1
Input Low Current	I _{IL1}	V _{IN} = 0 V; Inputs with no pull-up resistors	-5			uA	1
	I _{IL2}	V _{IN} = 0 V; Inputs with pull-up resistors	-200			uA	1
Low Threshold Input-High Voltage	V _{IH_FSL}	3.3 V +/-5%	0.7		V _{DD} + 0.3	V	1
Low Threshold Input-Low Voltage	V _{IL_FSL}	3.3 V +/-5%	V _{SS} - 0.3		0.35	V	1
Operating Supply Current	I _{DD3.3OP}	Full Active, C _L = Full load;			350	mA	1
Operating Current	I _{DD3.3OP}	all outputs driven			400	mA	1
Powerdown Current	I _{DD3.3PD}	all diff pairs driven			70	mA	1
		all differential pairs tri-stated			12	mA	1
Input Frequency	F _i	V _{DD} = 3.3 V		14.31818		MHz	2
Pin Inductance	L _{pin}				7	nH	1
Input Capacitance	C _{IN}	Logic Inputs			5	pF	1
	C _{OUT}	Output pin capacitance			6	pF	1
	C _{INX}	X1 & X2 pins			5	pF	1
Clk Stabilization	T _{STAB}	From V _{DD} Power-Up or de-assertion of PD# to 1st clock			1.8	ms	1
Modulation Frequency		Triangular Modulation	30		33	kHz	1
Tdrive_PD#		CPU output enable after PD# de-assertion			300	us	1
Tfall_Pd#		PD# fall time of			5	ns	1
Trise_Pd#		PD# rise time of			5	ns	1
SMBus Voltage	V _{DD}		2.7		5.5	V	1
Low-level Output Voltage	V _{OL}	@ I _{PULLUP}			0.4	V	1
Current sinking at V _{OL} = 0.4 V	I _{PULLUP}		4			mA	1
SCLK/SDATA Clock/Data Rise Time	T _{RI2C}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Clock/Data Fall Time	T _{FI2C}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%

¹Guaranteed by design and characterization, not 100% tested in production.

² Input frequency should be measured at the REF pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.

Electrical Characteristics - CPUCLKT/C -- 0.7V Current Mode Differential Pair

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Current Source Output Impedance	Z _o	V _O = V _x	3000			Ω	1
Voltage High	V _{High}	Statistical measurement on single ended signal	660		850	mV	1,3
Voltage Low	V _{Low}		-150		150	mV	1,3
Max Voltage	V _{ovs}	Measurement on single ended signal using absolute value.			1150	mV	1
Min Voltage	V _{uds}		-300			mV	1
Crossing Voltage (abs)	V _{x(abs)}		250		550	mV	1
Crossing Voltage (var)	d-V _x	Variation of crossing over all edges			140	mV	1
Long Accuracy	ppm	see T _{period} min-max values	-300		300	ppm	1,2
Average period	T _{period}	400MHz nominal	2.4993		2.5008	ns	2
		400MHz spread	2.4993		2.5133	ns	2
		333.33MHz nominal	2.9991		3.0009	ns	2
		333.33MHz spread	2.9991		3.016	ns	2
		266.66MHz nominal	3.7489		3.7511	ns	2
		266.66MHz spread	3.7489		3.77	ns	2
		200MHz nominal	4.9985		5.0015	ns	2
		200MHz spread	4.9985		5.0266	ns	2
		166.66MHz nominal	5.9982		6.0018	ns	2
		166.66MHz spread	5.9982		6.0320	ns	2
		133.33MHz nominal	7.4978		7.5023	ns	2
		133.33MHz spread	7.4978		7.5400	ns	2
		100.00MHz nominal	9.9970		10.0030	ns	2
		100.00MHz spread	9.9970		10.0533	ns	2
Absolute min period	T _{absmin}	400MHz nominal/spread	2.4143			ns	1,2
		333.33MHz nominal/spread	2.9141			ns	1,2
		266.66MHz nominal/spread	3.6639			ns	1,2
		200MHz nominal/spread	4.8735			ns	1,2
		166.66MHz nominal/spread	5.8732			ns	1,2
		133.33MHz nominal/spread	7.3728			ns	1,2
		100.00MHz nominal/spread	9.8720			ns	1,2
Rise Time	t _r	V _{OL} = 0.175V, V _{OH} = 0.525V	175		700	ps	1
Fall Time	t _f	V _{OH} = 0.525V V _{OL} = 0.175V	175		700	ps	1
Rise Time Variation	d-t _r	V _{OL} = 0.175V, V _{OH} = 0.525V			125	ps	1
Fall Time Variation	d-t _f	V _{OH} = 0.525V V _{OL} = 0.175V			125	ps	1
Duty Cycle	d ₁₃	Measurement from differential waveform	45		55	%	1
Skew	t _{sk3}	CPU(1:0), V _T = 50%			100	ps	1
Skew	t _{sk4}	CPU(1:0) to CPU2_ITP, V _T = 50%			150	ps	1
Jitter, Cycle to cycle	t _{j cyc-cyc}	Measurement from differential waveform (CPU2_ITP)			125	ps	1
Jitter, Cycle to cycle	t _{j cyc-cyc}	Measurement from differential waveform, (CPU(1:0))			85	ps	1

*T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =2pF, R_S=33.2Ω, R_P=49.9Ω, I_{REF} = 475Ω

¹Guaranteed by design and characterization, not 100% tested in production.

² All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

³I_{REF} = V_{DD}/(3xR_R). For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω.

Electrical Characteristics - SRC/SATA/PCIEX 0.7V Current Mode Differential Pair

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	Notes
Current Source Output Impedance	Z _o	V _O = V _x	3000			Ω	1
Voltage High	V _{High}	Statistical measurement on single ended signal	660		850	mV	1,3
Voltage Low	V _{Low}		-150		150	mV	1,3
Max Voltage	V _{ovs}	Measurement on single ended signal using absolute value.			1150	mV	1
Min Voltage	V _{uds}		-300			mV	1
Crossing Voltage (abs)	V _{x(abs)}		250		550	mV	1
Crossing Voltage (var)	d-V _x	Variation of crossing over all edges			140	mV	1
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Average period	Tperiod	100.00MHz nominal	9.9970		10.0030	ns	2
		100.00MHz spread	9.9970		10.0533	ns	2
Absolute min period	Tabmin	100.00MHz nominal/spread	9.8720			ns	1,2
Rise Time	t _r	V _{OL} = 0.175V, V _{OH} = 0.525V	175		700	ps	1
Fall Time	t _f	V _{OH} = 0.525V V _{OL} = 0.175V	175		700	ps	1
Rise Time Variation	d-t _r	V _{OL} = 0.175V, V _{OH} = 0.525V			125	ps	1
Fall Time Variation	d-t _f	V _{OH} = 0.525V V _{OL} = 0.175V			125	ps	1
Duty Cycle	d _{t3}	Measurement from differential waveform	45		55	%	1
Skew	t _{sk3}	V _T = 50%			250	ps	1
Jitter, Cycle to cycle	t _{jcy-cyc}	Measurement from differential waveform			125	ps	1

*T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L = 2pF, R_S = 33.2Ω, R_P = 49.9Ω, I_{REF} = 475Ω

¹Guaranteed by design and characterization, not 100% tested in production.

² All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

³I_{REF} = V_{DD}/(3xR_P). For R_P = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O = 50Ω.

Electrical Characteristics - PCICLK/PCICLK_F

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Output Impedance	R _{DSP}	V _O = V _{DD} *(0.5)	12		55	Ω	1
Output High Voltage	V _{OH}	I _{OH} = -1 mA	2.4			V	1
Output Low Voltage	V _{OL}	I _{OL} = 1 mA			0.55	V	1
Output High Current	I _{OH}	V _{OH} @ MIN = 1.0 V	-33			mA	1
		V _{OH} @ MAX = 3.135 V			-33	mA	1
Output Low Current	I _{OL}	V _{OL} @ MIN = 1.95 V	30			mA	1
		V _{OL} @ MAX = 0.4 V			38	mA	1
Edge Rate	t _{slewrf}	Rising/Falling edge rate	1		4	V/ns	1
Rise Time	t _r	V _{OL} = 0.4 V, V _{OH} = 2.4 V	0.5		2	ns	1
Fall Time	t _f	V _{OH} = 2.4 V, V _{OL} = 0.4 V	0.5		2	ns	1
Duty Cycle	d _{t1}	V _T = 1.5 V	45		55	%	1
Group Skew	t _{skew}	V _T = 1.5 V			500	ps	1
Jitter, Cycle to cycle	t _{jcy-cyc}	V _T = 1.5 V			250	ps	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 20 pF with Rs = 7Ω (unless otherwise specified)

¹Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - 48MHz/USB48MHz/24_48MHz

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-100		100	ppm	1
Clock period	T _{period}	48.00MHz output nominal	20.8313		20.8354	ns	
Output Impedance	R _{DSP}	V _O = V _{DD} *(0.5)	12		55	Ω	1
Output High Voltage	V _{OH}	I _{OH} = -1 mA	2.4			V	1
Output Low Voltage	V _{OL}	I _{OL} = 1 mA			0.55	V	1
Output High Current	I _{OH}	V _{OH} @ MIN = 1.0 V	-33			mA	1
		V _{OH} @ MAX = 3.135 V			-33	mA	1
Output Low Current	I _{OL}	V _{OL} @ MIN = 1.95 V	30			mA	1
		V _{OL} @ MAX = 0.4 V			38	mA	1
Edge Rate	t _{slewrif}	Rising/Falling edge rate	1		4	V/ns	1
Edge Rate	t _{slewrif_USB}	USB48 Rising/Falling edge rate	1		2	V/ns	1
Rise Time	t _r	V _{OL} = 0.4 V, V _{OH} = 2.4 V	0.5		2	ns	1
Fall Time	t _f	V _{OH} = 2.4 V, V _{OL} = 0.4 V	0.5		2	ns	1
Rise Time	t _{r_USB}	V _{OL} = 0.4 V, V _{OH} = 2.4 V	1		2	ns	1
Fall Time	t _{f_USB}	V _{OH} = 2.4 V, V _{OL} = 0.4 V	1		2	ns	1
Duty Cycle	d _{TI}	V _T = 1.5 V	45		55	%	1
Jitter, Cycle to cycle	t _{jyc-cyc}	V _T = 1.5 V			500	ps	1

*T_A = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 20 pF with Rs = 7Ω (Rs is used in USB48MHz test only)

¹Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - DOT_96MHz 0.7V Current Mode Differential Pair

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	Notes
Current Source Output Impedance	Z _o	V _O = V _x	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal	660		850	mV	1,3
Voltage Low	VLow		-150		150	mV	1,3
Max Voltage	Vovs	Measurement on single ended signal using absolute value.			1150	mV	1
Min Voltage	Vuds		-300			mV	1
Crossing Voltage (abs)	Vx(abs)		250		550	mV	1
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges			140	mV	1
Long Accuracy	ppm	see Tperiod min-max values	-100		100	ppm	1,2
Average period	Tperiod	96.00MHz nominal	10.4135		10.4198	ns	2
Absolute min period	Tabsmin	96.00MHz nominal	10.1635			ns	1,2
Rise Time	t _r	V _{OL} = 0.175V, V _{OH} = 0.525V	175		700	ps	1
Fall Time	t _f	V _{OH} = 0.525V V _{OL} = 0.175V	175		700	ps	1
Rise Time Variation	d-t _r	V _{OL} = 0.175V, V _{OH} = 0.525V			125	ps	1
Fall Time Variation	d-t _f	V _{OH} = 0.525V V _{OL} = 0.175V			125	ps	1
Duty Cycle	d _{IS}	Measurement from differential waveform	45		55	%	1
Jitter, Cycle to cycle	t _{jyc-cyc}	Measurement from differential waveform			250	ps	1

*T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L = 2pF, R_S = 33.2Ω, R_P = 49.9Ω, I_{REF} = 475Ω

¹Guaranteed by design and characterization, not 100% tested in production.

² All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

³I_{REF} = V_{DD}/(3xR_P). For R_P = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O = 50Ω.

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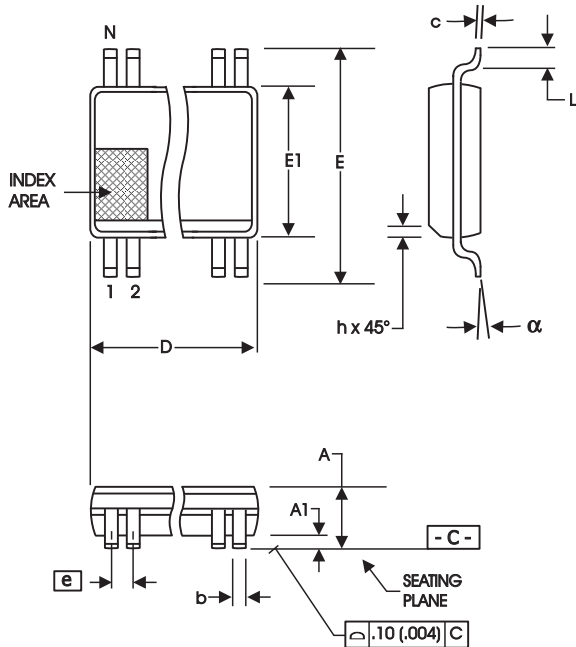
Electrical Characteristics - REF-14.318MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see T _{period} min-max values	-300		300	ppm	1,2
Clock period	T _{period}	14.318MHz output nominal	69.8270		69.8550	ns	2
Output High Voltage	V _{OH}	I _{OH} = -1 mA	2.4			V	1
Output Low Voltage	V _{OL}	I _{OL} = 1 mA			0.4	V	1
Output High Current	I _{OH}	V _{OH} @MIN = 1.0 V, V _{OH} @MAX = 3.135 V	-29		-23	mA	1
Output Low Current	I _{OL}	V _{OL} @MIN = 1.95 V, V _{OL} @MAX = 0.4 V	29		27	mA	1
Edge Rate	t _{slewrf}	Rising/Falling edge rate	1		4	V/ns	1
Rise Time	t _{r1}	V _{OL} = 0.4 V, V _{OH} = 2.4 V	1		2	ns	1
Fall Time	t _{f1}	V _{OH} = 2.4 V, V _{OL} = 0.4 V	1		2	ns	1
Duty Cycle	d _{t1}	V _T = 1.5 V	45		55	%	1
Jitter	t _{jyc-cyc}	V _T = 1.5 V			1000	ps	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 20 pF with Rs = 7Ω (Rs is used in USB48MHz test only)

¹Guaranteed by design and characterization, not 100% tested in production.

² All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz



56-Lead, 300 mil Body, 25 mil, SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	18.31	18.55	.720	.730

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

954119yFLF-T

Example:

XXXX y F LF-T

Designation for tape and reel packaging

Lead Free (Optional)

Package Type
F = SSOP

Revision Designator (will not correlate with datasheet revision)

Device Type