0.5 GHz to 4.0 GHz, GaAs, SPST Switch

Data Sheet **HMC1055**

FEATURES

Low insertion loss: 0.7 dB typical at 2.0 GHz
High input third-order intercept (IP3): >60 dBm typical
Single positive control: 0 V or 3 V
Small, surface-mount, 8-lead, 2 mm × 2 mm LFCSP package

APPLICATIONS

Cellular infrastructure
Wireless infrastructure
Mobile radios
Test equipment

FUNCTIONAL BLOCK DIAGRAM

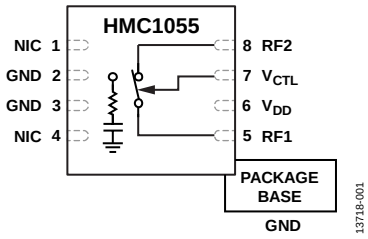

Figure 1.

GENERAL DESCRIPTION

The HMC1055 is a low cost, gallium arsenide (GaAs), single-pole, single-throw (SPST) switch in a surface-mount LFCSP package. This switch offers low insertion loss, high isolation, and exceptional third-order intermodulation performance that make it ideal for many cellular and wireless infrastructure applications from 0.5 GHz to 4.0 GHz.

The HMC1055 operates with single positive supply voltage and a single positive control voltage at very low dc currents. RF1 is reflective open, whereas RF2 is terminated to 50 Ω in the off state.

Rev. B **Document Feedback**

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support **www.analog.com**

TABLE OF CONTENTS

REVISION HISTORY

8/2018—Rev. A to Rev. B

Changes to Reflow Temperature Parameter, Table 2 ... 4
Updated Outline Dimensions ... 10
Changes to Ordering Guide ... 10

2/2016—v00.0912 to Rev. A

This Hittite Microwave Products data sheet has been reformatted to meet the styles and standards of Analog Devices, Inc.

Changed NC to NIC ... Throughout
Changes to Title, Features Section, Applications Section, Figure 1, and General Description Section ... 1
Changes to Table 1 ... 3
Changes to Table 2 ... 4
Added Figure 2; Renumbered Sequentially ... 5
Changes to Table 3 ... 5
Deleted Typical Application Circuit ... 5
Changes to Figure 5 ... 6
Changes to Figure 11 and Figure 12 ... 7
Changes to Theory of Operation Section and Table 4 ... 8
Added Applications Information Section, Evaluation Printed Circuit Board Section, Evaluation Board Schematic and Artwork Section, and Figure 13; Renumbered Sequentially ... 9
Changes to Table 5 ... 9
Updated Outline Dimensions ... 10
Changes to Ordering Guide ... 10

SPECIFICATIONS

V_{DD} = 3 V , V_{CTL} = 0 V or V_{DD}, T_A = 25°C, 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY		0.5		4.0	GHz
INSERTION LOSS	0.5 GHz to 2.0 GHz		0.7		dB
	2.0 GHz to 4.0 GHz		1.4		dB
ISOLATION	0.5 GHz to 2.0 GHz		36		dB
	2.0 GHz to 4.0 GHz		28		dB
RETURN LOSS					
On State	0.5 GHz to 2.0 GHz, RF1 and RF2 ports		27		dB
	2.0 GHz to 4.0 GHz, RF1 and RF2 ports		25		dB
Off State	0.5 GHz to 2.0 GHz, RF2 port		12		dB
	2.0 GHz to 4.0 GHz, RF2 port		24		dB
INPUT LINEARITY	0.5 GHz to 4.0 GHz				
Input 0.1 dB Compression (P0.1dB)			28		dBm
Input Third-Order Intercept (IP3)	Two-tone input power = 15 dBm each tone		>60		dBm
SWITCHING CHARACTERISTICS					
Rise/Fall Time (t_{RISE}, t_{FALL})	10% to 90% RF		40		ns
On/Off Time (t_{ON}, t_{OFF})	50% V_{CTL} to 90% RF		50		ns
CURRENT					
Supply (I_{DD})	V_{DD} = 3 V to 5 V		0.2		mA
Control (I_{CTL})	0 V or V_{DD}		<5		µA

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
RF Input Power (V_{DD} = 3 V, T_{CASE} = 85°C)	34 dBm
Supply Voltage	6.0 V
Control Voltage Range	−0.2 V to V_{DD} + 0.2 V
Continuous Power Dissipation, P_{DISS}	0.88 W
Thermal Resistance, θ_{JC} (Channel to Package Bottom)	74°C/W
Channel Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Reflow Temperature	260°C
ESD Sensitivity, Human Body Model (HBM)	250 V (Class 1A)

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

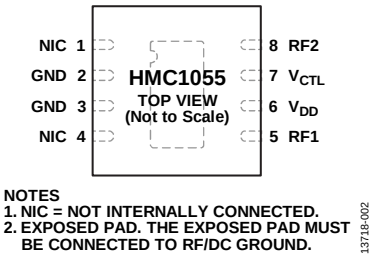

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 4	NIC	Not Internally Connected. These pins are not internally connected but can be grounded.
2, 3	GND	Ground. These pins must be connected to RF ground.
5	RF1	RF Input. This pin is dc-coupled and matched to 50 Ω. A blocking capacitor is required.
6	V_{DD}	Supply Voltage Pin.
7	V_{CTL}	Control Input Pin.
8	RF2	RF Output. This pin is dc-coupled and matched to 50 Ω. A blocking capacitor is required.
	EPAD	Exposed Pad. The exposed pad must be connected to RF/dc ground.

INTERFACE SCHEMATICS

Figure 3. GND Interface Schematic

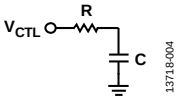

Figure 4. V_{CTL} Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

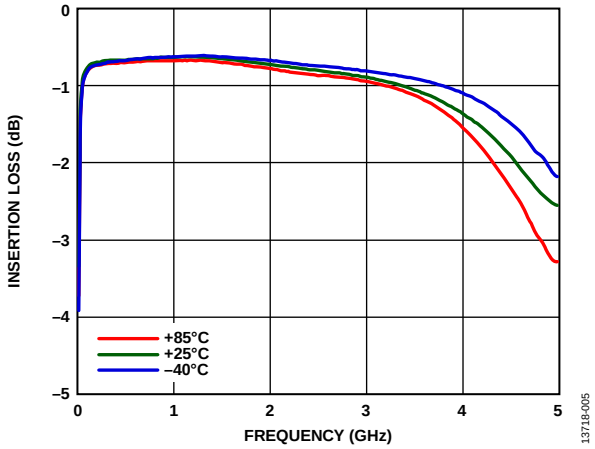

Figure 5. Insertion Loss vs. Frequency over Temperature, V_{DD} = 3 V, V_{CTL} = 3 V

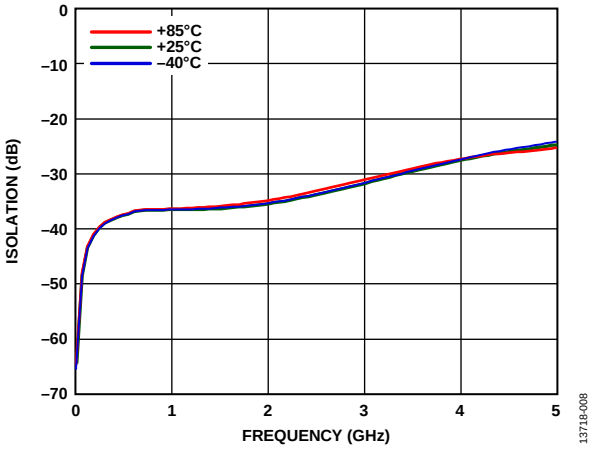

Figure 8. Isolation vs. Frequency over Temperature, V_{DD} = 3 V, V_{CTL} = 0 V

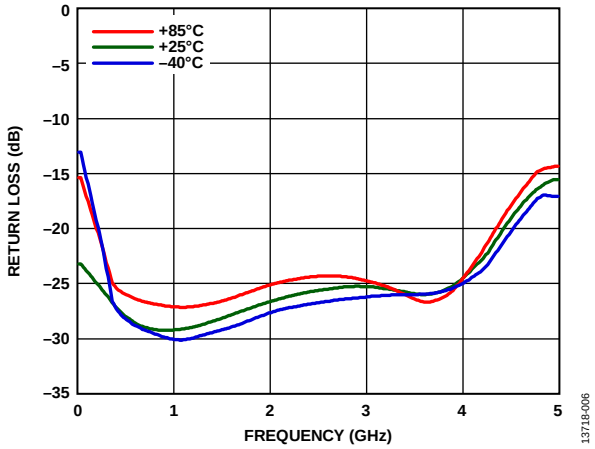

Figure 6. RF1 Return Loss vs. Frequency over Temperature, V_{DD} = 3 V, V_{CTL} = 3 V

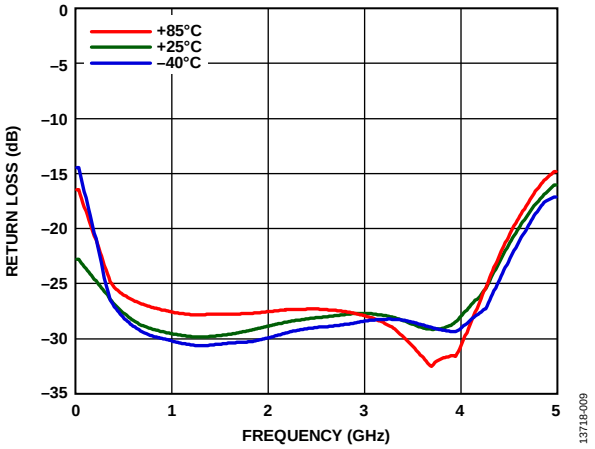

Figure 9. RF2 Return Loss vs. Frequency over Temperature, V_{DD} = 3 V, V_{CTL} = 3 V

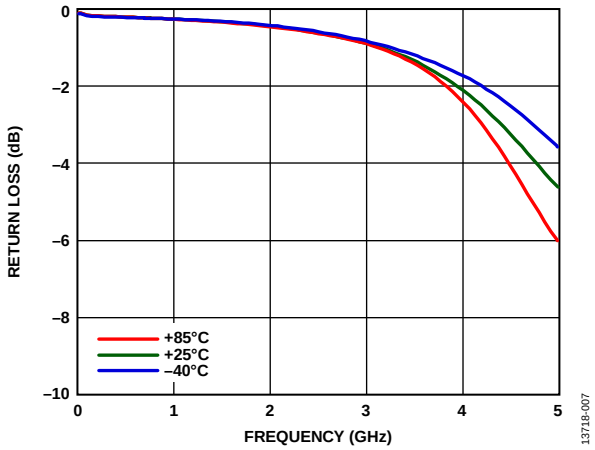

Figure 7. RF1 Return Loss vs. Frequency over Temperature, V_{DD} = 3 V, V_{CTL} = 0 V

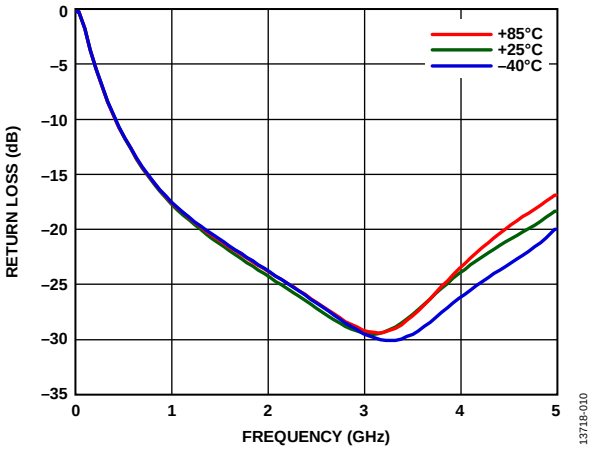

Figure 10. RF2 Return Loss vs. Frequency over Temperature, V_{DD} = 3 V, V_{CTL} = 0 V

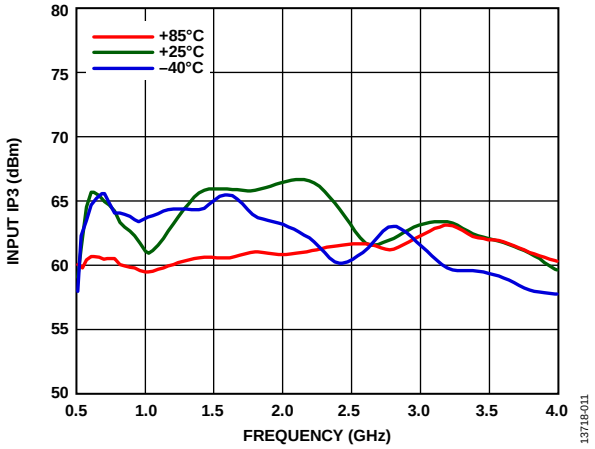

Figure 11. Input IP3 vs. Frequency Over Temperature, V_{DD} = 3 V, V_{CTL} = 3 V

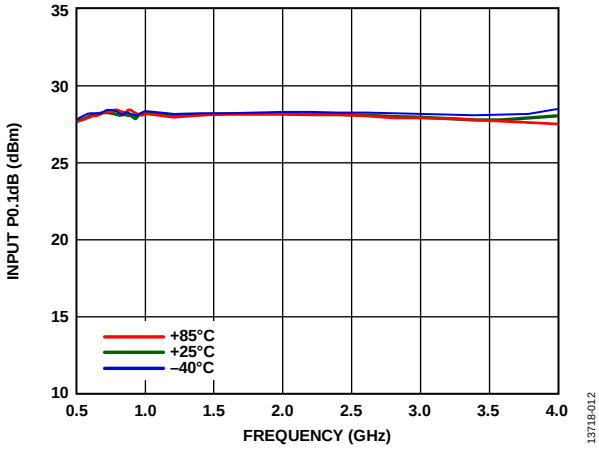

Figure 12. Input P0.1dB vs. Frequency Over Temperature, V_{DD} = 3 V, V_{CTL} = 3 V

THEORY OF OPERATION

The HMC1055 requires a single-supply voltage applied to the V_{DD} pin. Bypassing capacitors are recommended on the supply line to minimize RF coupling.

The HMC1055 is controlled via a single digital control voltage applied to the V_{CTL} pin. When the V_{CTL} pin is high, the switch is set to the on state, by which an insertion loss path is provided from RF1 to RF2. When the V_{CTL} pin is low, the switch is set to the off state, by which RF2 is isolated from RF1 and terminated to 50 Ω, whereas RF1 becomes reflective open (see Table 4).

The HMC1055 is internally matched to 50 Ω at the RF1 and RF2 pins; therefore, no external matching components are required. The RF1 and RF2 pins are dc-coupled, and dc blocking capacitors are required on the RF lines.

Table 4. Truth Table

Supply Voltage (V_{DD})	Control Voltage (V_{CTL})[1]	Switch Mode (RF1 to RF2)
3 V	0 V	Off
	3 V	On
5 V	0 V	Off
	5 V	On

[1] Control voltage tolerances are ±0.2 V dc.

APPLICATIONS INFORMATION

EVALUATION PRINTED CIRCUIT BOARD (PCB)

The HMC1055 evaluation board is constructed of a 4-layer material with a copper thickness of 0.7 mil on each layer. Every copper layer is separated with a dielectric material. The top dielectric material is 10 mil RO4350. The middle and bottom dielectric materials are FR-4, used for mechanical strength and overall board thickness of approximately 62 mil, which allows SMA connectors to be slipped in at the board edges.

All RF and dc traces are routed on the top copper layer. The RF transmission lines are designed using a coplanar waveguide (CPWG) model, with a width of 16 mil, spacing of 13 mil, and dielectric thickness of 10 mil, to have a characteristic impedance of 50 Ω. The inner and bottom layers are grounded planes to provide a solid ground for the RF transmission lines. For optimal electrical and thermal performance, as many vias as possible are arranged around the transmission lines and under the package exposed pad. The evaluation board layout shown in Figure 14 serves as a recommendation for optimal and stable performance, as well as for improvement of thermal efficiency.

The package ground pins are connected directly to the ground plane. The supply voltage and control voltage must be connected to the dc pins, J3 and J4, respectively, of the evaluation board. One decoupling capacitor is populated on the supply trace to filter high frequency noise.

The RF input and output ports (RF1 and RF2) are connected through 50 Ω transmission lines to the SMA connectors, J1 and J2, respectively. The RF1 and RF2 ports are ac-coupled with capacitors of an appropriate value to ensure broadband performance. A thru calibration line connects J5 and J6; this transmission line is used to estimate the loss of the PCB over the environmental conditions being evaluated.

EVALUATION BOARD SCHEMATIC AND ARTWORK

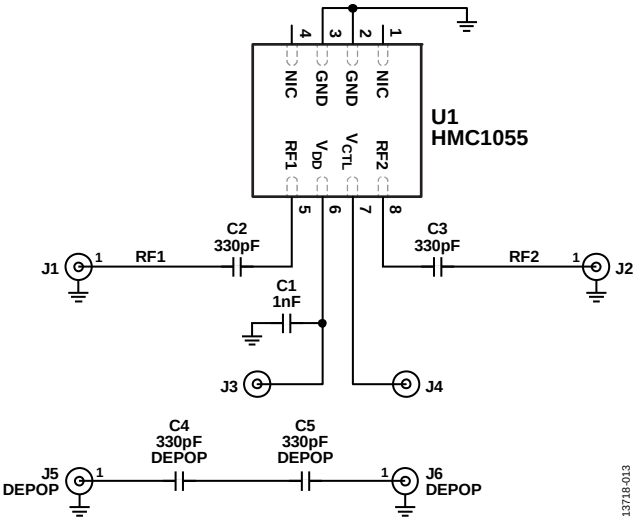

Figure 13. Evaluation Board Schematic

Table 5. List of Materials for EVAL01-HMC1055LP2C

Item	Description
J1, J2	PCB mount, SMA, RF connector
J3, J4	DC pin
C1	1 nF capacitor, 0402 package
C2, C3	330 pF capacitor, 0402 package
U1	HMC1055 SPST switch
PCB	600-00215-00-1 evaluation PCB

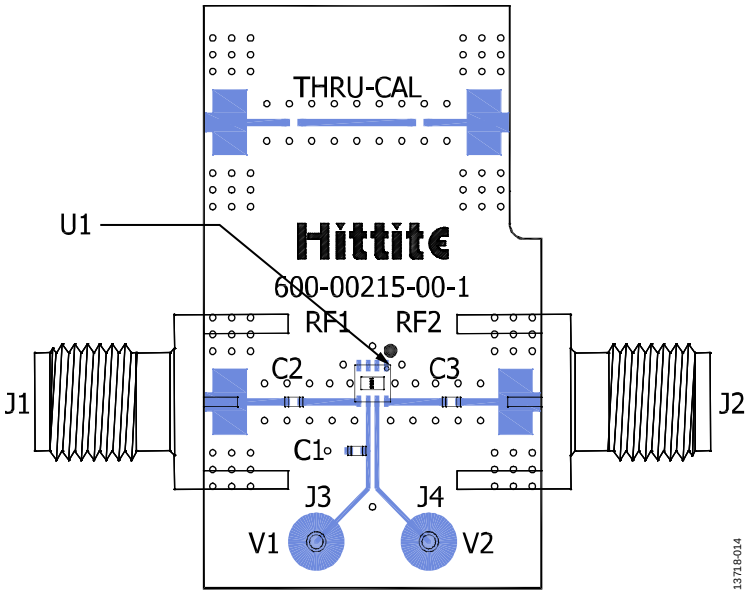

Figure 14. Evaluation Board Layout—Top View

OUTLINE DIMENSIONS

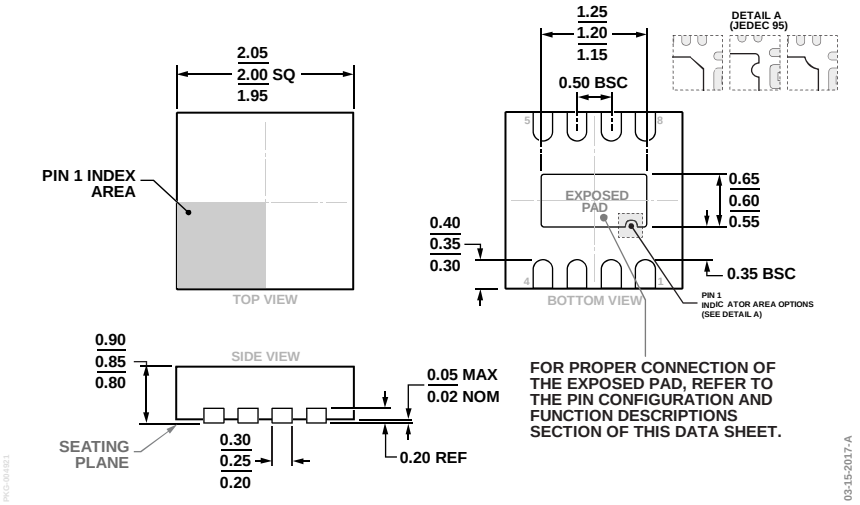

Figure 15. 8-Lead Lead Frame Chip Scale Package [LFCSP]
2 mm × 2 mm Body and 0.90 mm Package Height
(CP-8-26)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
HMC1055LP2CE	−40°C to +85°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-26
HMC1055LP2CETR	−40°C to +85°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-26
EVAL01-HMC1055LP2C		Evaluation Board	

[1] All models are RoHS compliant.

D13718-0-8/18(B)