2nd Generation Intel® Core™ Processor Family Desktop, Intel® Pentium® Processor Family Desktop, and Intel® Celeron® Processor Family Desktop

Datasheet, Volume 1

Supporting Intel® Core™ i7, i5, and i3 Desktop Processor Series

Supporting Intel® Pentium® Processor G800 and G600 Series

Supporting Intel® Celeron® Processor G500 and G400 Series

This is Volume 1 of 2

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Revision History

Revision Number	Description	Revision Date
001	Initial release	January 2011
002	• Added Intel® Core™ i5-2405S, i5-2310, and i3-2105 processors • Added Intel® Pentium® processor family desktop – Intel® Pentium® G850, G840, G620, and G620T processors	May 2011
003	• Added Intel® Core™ i5-2320, i3-2125, i3-2130, and i3-2120T processors • Added Intel® Celeron® processor family desktop – Intel® Celeron G540, G530, G530T, and G440 processors • Added Intel® Pentium® G860, G630, and G630T processors	September 2011
004	• Added Intel® Core™ i7-2700K processor	October 2011
005	• Added Intel® Celeron® G460 processor	December 2011
006	• Added Intel® Core™ i5-2550K, i5-2450P, i5-2380P processors	January 2012
007	• Added Intel® Pentium® G645, G645T processors • Added Intel® Celeron® G555, G550T, G465 processors	September 2012
008	• Added Intel® Celeron® G470 processors	June 2013

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1 Introduction

The 2nd Generation Intel® Core™ processor family desktop, Intel® Pentium® processor family desktop, and Intel® Celeron® processor family desktop are the next generation of 64-bit, multi-core desktop processor built on 32- nanometer process technology. Based on a new micro-architecture, the processor is designed for a two-chip platform consisting of a processor and Platform Controller Hub (PCH). The platform enables higher performance, lower cost, easier validation, and improved x-y footprint. The processor includes Integrated Display Engine, Processor Graphics, PCI Express* ports, and Integrated Memory Controller. The processor is designed for desktop platforms. It supports up to 12 Processor Graphics execution units (EUs). The processor is offered in an 1155-land LGA package. Figure 1-1 shows an example desktop platform block diagram.

This document provides DC electrical specifications, signal integrity, differential signaling specifications, pinout and signal definitions, interface functional descriptions, thermal specifications, and additional feature information pertinent to the implementation and operation of the processor on its respective platform.

Note: Throughout this document, 2nd Generation Intel® Core™ processor family desktop, Intel® Pentium® processor family desktop, and Intel® Celeron® processor family desktop may be referred to as simply the processor.

Note: Throughout this document, the Intel® Core™ i7 desktop processor series refers to the Intel® Core™ i7-2700K, i7-2600K, i7-2600S, and i7-2600 processors.

Note: Throughout this document, the Intel® Core™ i5 desktop processor series refers to the Intel® Core™ i5-2550K, i5-2500K, i5-2500S, i5-2500T, i5-2500, i5-2450P, i5-2400, i5-2405S, i5-2400S, i5-2390T, i5-2380P, i5-2320, i5-2310, and i5-2300 processors.

Note: Throughout this document, the Intel® Core™ i3 desktop processor series refers to the Intel® Core™ i3-2130, i3-2125, i3-2120, i3-2120T, i3-2105, i3-2100, and i3-2100T processors.

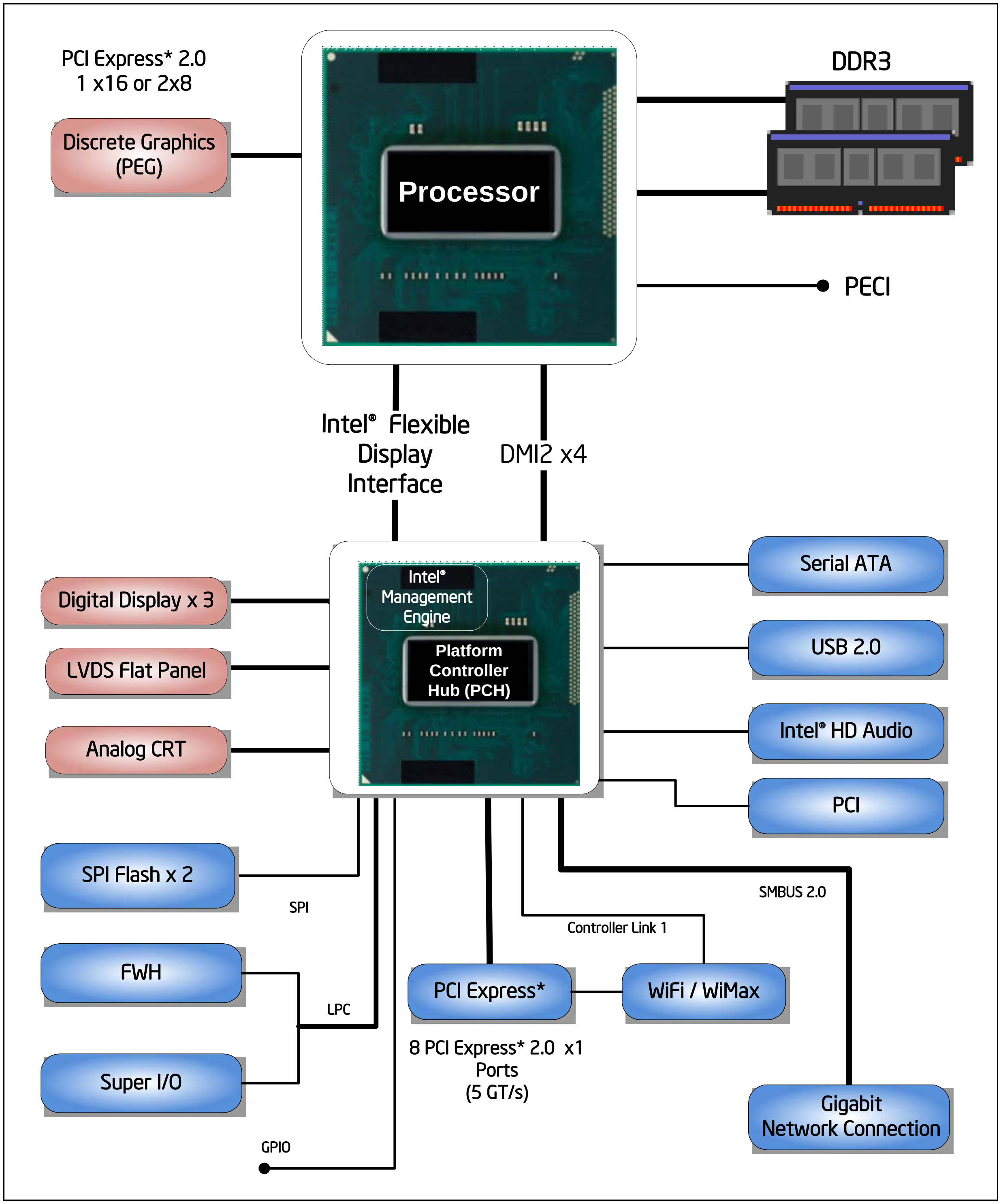
Note: Throughout this document, the Intel® Pentium® processor family desktop refers to the Intel® Pentium® G870, G860, G860T, G850, G840, G645, G645T, G640, G540T, G630, G630T, G620, and G620T processors.

Throughout this document, the Intel® Celeron® processor family desktop refers to the Intel® Celeron® G555, G550, G550T, G540, G540T, G530, G530T, G470, G465, G460, and G440 processors.

Note: Throughout this document, the Intel® 6 Series Chipset Platform Controller Hub may also be referred to as “PCH”.

Note: Some processor features are not available on all platforms. Refer to the processor specification update for details.

Figure 1-1. Desktop Platform System Block Diagram Example



1.1 Processor Feature Details

- Four or two execution cores
- A 32-KB instruction and 32-KB data first-level cache (L1) for each core
- A 256-KB shared instruction/data second-level cache (L2) for each core
- Up to 8-MB shared instruction/data third-level cache (L3), shared among all cores

1.1.1 Supported Technologies

- Intel® Virtualization Technology (Intel® VT) for Directed I/O (Intel® VT-d)
- Intel® Virtualization Technology (Intel® VT) for IA-32, Intel® 64 and Intel® Architecture (Intel® VT-x)
- Intel® Active Management Technology 7.0 (Intel® AMT 7.0)
- Intel® Trusted Execution Technology (Intel® TXT)
- Intel® Streaming SIMD Extensions 4.1 (Intel® SSE4.1)
- Intel® Streaming SIMD Extensions 4.2 (Intel® SSE4.2)
- Intel® Hyper-Threading Technology (Intel® HT Technology)
- Intel® 64 Architecture
- Execute Disable Bit
- Intel® Turbo Boost Technology
- Intel® Advanced Vector Extensions (Intel® AVX)
- Intel® Advanced Encryption Standard New Instructions (Intel® AES-NI)
- PCLMULQDQ Instruction

1.2 Interfaces

1.2.1 System Memory Support

- Two channels of unbuffered DDR3 memory with a maximum of two UDIMMs or SO-DIMMs (for AIO) per channel
- Single-channel and dual-channel memory organization modes
- Data burst length of eight for all memory organization modes
- Memory DDR3 data transfer rates of 1066 MT/s and 1333 MT/s
- 64-bit wide channels
- DDR3 I/O Voltage of 1.5 V
- The type of memory supported by the processor is dependent on the PCH SKU in the target platform
    - Desktop PCH platforms support non-ECC un-buffered DIMMs only
    - All In One platforms (AIO) support SO-DIMMs
- Maximum memory bandwidth of 10.6 GB/s in single-channel mode or 21 GB/s in dual-channel mode assuming DDR3 1333 MT/s
- 1Gb, 2Gb, and 4Gb DDR3 DRAM technologies are supported
    - Using 4Gb device technologies, the largest memory capacity possible is 32 GB, assuming Dual Channel Mode with four x8 dual ranked unbuffered DIMM memory configuration.

- Up to 64 simultaneous open pages, 32 per channel (assuming 8 ranks of 8 bank devices)
- Command launch modes of 1n/2n
- On-Die Termination (ODT)
- Asynchronous ODT
- Intel® Fast Memory Access (Intel® FMA)
  - Just-in-Time Command Scheduling
  - Command Overlap
  - Out-of-Order Scheduling

1.2.2 PCI Express*

- PCI Express* port(s) are fully-compliant with the *PCI Express Base Specification, Revision 2.0*.
- Processor with desktop PCH supported configurations

Table 1-1. PCI Express* Supported Configurations in Desktop Products

Configuration	Organization	Desktop
1	2x8	Graphics, I/O
2	1x16	Graphics, I/O

- The port may negotiate down to narrower widths
  - Support for x16/x8/x4/x1 widths for a single PCI Express mode
- 2.5 GT/s and 5.0 GT/s PCI Express* frequencies are supported
- Gen1 Raw bit-rate on the data pins of 2.5 GT/s, resulting in a real bandwidth per pair of 250 MB/s given the 8b/10b encoding used to transmit data across this interface. This also does not account for packet overhead and link maintenance.
- Maximum theoretical bandwidth on the interface of 4 GB/s in each direction simultaneously, for an aggregate of 8 GB/s when x16 Gen 1
- Gen 2 Raw bit-rate on the data pins of 5.0 GT/s, resulting in a real bandwidth per pair of 500 MB/s given the 8b/10b encoding used to transmit data across this interface. This also does not account for packet overhead and link maintenance.
- Maximum theoretical bandwidth on the interface of 8 GB/s in each direction simultaneously, for an aggregate of 16 GB/s when x16 Gen 2
- Hierarchical PCI-compliant configuration mechanism for downstream devices
- Traditional PCI style traffic (asynchronous snooped, PCI ordering)
- PCI Express* extended configuration space. The first 256 bytes of configuration space aliases directly to the PCI Compatibility configuration space. The remaining portion of the fixed 4-KB block of memory-mapped space above that (starting at 100h) is known as extended configuration space.
- PCI Express* Enhanced Access Mechanism; accessing the device configuration space in a flat memory mapped fashion
- Automatic discovery, negotiation, and training of link out of reset
- Traditional AGP style traffic (asynchronous non-snooped, PCI-X Relaxed ordering)
- Peer segment destination posted write traffic (no peer-to-peer read traffic) in Virtual Channel 0
  - DMI -> PCI Express* Port 0

- 64-bit downstream address format, but the processor never generates an address above 64 GB (Bits 63:36 will always be zeros)
- 64-bit upstream address format, but the processor responds to upstream read transactions to addresses above 64 GB (addresses where any of Bits 63:36 are nonzero) with an Unsupported Request response. Upstream write transactions to addresses above 64 GB will be dropped.
- Re-issues Configuration cycles that have been previously completed with the Configuration Retry status
- PCI Express* reference clock is 100-MHz differential clock
- Power Management Event (PME) functions
- Dynamic width capability
- Message Signaled Interrupt (MSI and MSI-X) messages
- Polarity inversion

Note: The processor does not support PCI Express* Hot-Plug.

1.2.3 Direct Media Interface (DMI)

- DMI 2.0 support
- Four lanes in each direction
- 5 GT/s point-to-point DMI interface to PCH is supported
- Raw bit-rate on the data pins of 5.0 GB/s, resulting in a real bandwidth per pair of 500 MB/s given the 8b/10b encoding used to transmit data across this interface. Does not account for packet overhead and link maintenance.
- Maximum theoretical bandwidth on interface of 2 GB/s in each direction simultaneously, for an aggregate of 4 GB/s when DMI x4
- Shares 100-MHz PCI Express* reference clock
- 64-bit downstream address format, but the processor never generates an address above 64 GB (Bits 63:36 will always be zeros)
- 64-bit upstream address format, but the processor responds to upstream read transactions to addresses above 64 GB (addresses where any of Bits 63:36 are nonzero) with an Unsupported Request response. Upstream write transactions to addresses above 64 GB will be dropped.
- Supports the following traffic types to or from the PCH
    - DMI -> DRAM
    - DMI -> processor core (Virtual Legacy Wires (VLWs), Resetwarn, or MSIs only)
    - Processor core -> DMI
- APIC and MSI interrupt messaging support
    - Message Signaled Interrupt (MSI and MSI-X) messages
- Downstream SMI, SCI and SERR error indication
- Legacy support for ISA regime protocol (PHOLD/PHOLDA) required for parallel port DMA, floppy drive, and LPC bus masters
- DC coupling – no capacitors between the processor and the PCH
- Polarity inversion
- PCH end-to-end lane reversal across the link
- Supports Half Swing “low-power/low-voltage”

1.2.4 Platform Environment Control Interface (PECI)

The PECI is a one-wire interface that provides a communication channel between a PECI client (the processor) and a PECI master. The processors support the PECI 3.0 Specification.

1.2.5 Processor Graphics

- The Processor Graphics contains a refresh of the sixth generation graphics core enabling substantial gains in performance and lower power consumption.
- Next Generation Intel Clear Video Technology HD support is a collection of video playback and enhancement features that improve the end user's viewing experience.
    - Encode/transcode HD content
    - Playback of high definition content including Blu-ray Disc*
    - Superior image quality with sharper, more colorful images
    - Playback of Blu-ray disc S3D content using HDMI (V.1.4 with 3D)
- DirectX* Video Acceleration (DXVA) support for accelerating video processing
    - Full AVC/VC1/MPEG2 HW Decode
- Advanced Scheduler 2.0, 1.0, XPDM support
- Windows* 7, XP, Windows Vista*, OSX, Linux OS Support
- DX10.1, DX10, DX9 support
- OGL 3.0 support
- Switchable graphics support on desktop AIO platforms with MxM solutions only

1.2.6 Intel® Flexible Display Interface (Intel® FDI)

- For SKUs with graphics, Intel FDI carries display traffic from the Processor Graphics in the processor to the legacy display connectors in the PCH
- Based on DisplayPort standard
- Two independent links – one for each display pipe
- Four unidirectional downstream differential transmitter pairs
    - Scalable down to 3X, 2X, or 1X based on actual display bandwidth requirements
    - Fixed frequency 2.7 GT/s data rate
- Two sideband signals for Display synchronization
    - FDI_FSYNC and FDI_LSYNC (Frame and Line Synchronization)
- One Interrupt signal used for various interrupts from the PCH
    - FDI_INT signal shared by both Intel FDI Links
- PCH supports end-to-end lane reversal across both links
- Common 100-MHz reference clock

1.3 Power Management Support

1.3.1 Processor Core

- Full support of Advanced Configuration and Power Interface (ACPI) C-states as implemented by the following processor C-states
  - C0, C1, C1E, C3, C6
- Enhanced Intel SpeedStep® Technology

1.3.2 System

- S0, S3, S4, S5

1.3.3 Memory Controller

- Conditional self-refresh (Intel® Rapid Memory Power Management (Intel® RMPM))
- Dynamic power-down

1.3.4 PCI Express*

- L0s and L1 ASPM power management capability

1.3.5 Direct Media Interface (DMI)

- L0s and L1 ASPM power management capability

1.3.6 Processor Graphics Controller

- Intel® Rapid Memory Power Management (Intel® RMPM) – CxSR
- Intel® Graphics Performance Modulation Technology (Intel® GPMT)
- Intel Smart 2D Display Technology (Intel S2DDT)
- Graphics Render C-State (RC6)

1.4 Thermal Management Support

- Digital Thermal Sensor
- Intel Adaptive Thermal Monitor
- THERMTRIP# and PROCHOT# support
- On-Demand Mode
- Memory Thermal Throttling
- External Thermal Sensor (TS-on-DIMM and TS-on-Board)
- Render Thermal Throttling
- Fan speed control with DTS

1.5 Package

- The processor socket type is noted as LGA 1155. The package is a 37.5 x 37.5 mm Flip Chip Land Grid Array (FCLGA 1155).

Note: See the *2nd Generation Intel® Core™ Processor, Intel® Pentium® Processor, and Intel® Celeron® Processor, and LGA1155 Socket Thermal Mechanical Specifications and Design Guidelines* for complete details on package.

1.6 Terminology

Table 1-2. Terminology (Sheet 1 of 2)

Term	Description
ACPI	Advanced Configuration and Power Interface
AIO	All In One
BLT	Block Level Transfer
CRT	Cathode Ray Tube
DDR3	Third-generation Double Data Rate SDRAM memory technology
DMA	Direct Memory Access
DMI	Direct Media Interface
DP	DisplayPort*
DTS	Digital Thermal Sensor
Enhanced Intel SpeedStep® Technology	Technology that provides power management capabilities to laptops.
EU	Execution Unit
Execute Disable Bit	The Execute Disable bit allows memory to be marked as executable or non-executable, when combined with a supporting operating system. If code attempts to run in non-executable memory the processor raises an error to the operating system. This feature can prevent some classes of viruses or worms that exploit buffer overrun vulnerabilities and can thus help improve the overall security of the system. See the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* for more detailed information.
IMC	Integrated Memory Controller
Intel® 64 Technology	64-bit memory extensions to the IA-32 architecture
Intel® FDI	Intel® Flexible Display Interface
Intel® TXT	Intel® Trusted Execution Technology
Intel® Virtualization Technology	Processor virtualization which when used in conjunction with Virtual Machine Monitor software enables multiple, robust independent software environments inside a single platform.
Intel® VT-d	Intel® Virtualization Technology (Intel® VT) for Directed I/O. Intel VT-d is a hardware assist, under system software (Virtual Machine Manager or OS) control, for enabling I/O device virtualization. Intel VT-d also brings robust security by providing protection from errant DMAs by using DMA remapping, a key feature of Intel VT-d.
IOV	I/O Virtualization
ITPM	Integrated Trusted Platform Module
LCD	Liquid Crystal Display
LVDS	Low Voltage Differential Signaling. A high speed, low power data transmission standard used for display connections to LCD panels.
NCTF	Non-Critical to Function. NCTF locations are typically redundant ground or non-critical reserved, so the loss of the solder joint continuity at end of life conditions will not affect the overall product functionality.

Table 1-2. Terminology (Sheet 2 of 2)

Term	Description
PCH	Platform Controller Hub. The new, 2009 chipset with centralized platform capabilities including the main I/O interfaces along with display connectivity, audio features, power management, manageability, security and storage features.
PECI	Platform Environment Control Interface
PEG	PCI Express* Graphics. External Graphics using PCI Express* Architecture. A high-speed serial interface whose configuration is software compatible with the existing PCI specifications.
Processor	The 64-bit, single-core or multi-core component (package).
Processor Core	The term "processor core" refers to Si die itself which can contain multiple execution cores. Each execution core has an instruction cache, data cache, and 256-KB L2 cache. All execution cores share the L3 cache.
Processor Graphics	Intel® Processor Graphics
Rank	A unit of DRAM corresponding four to eight devices in parallel. These devices are usually, but not always, mounted on a single side of a SO-DIMM.
SCI	System Control Interrupt. Used in ACPI protocol.
Storage Conditions	A non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor landings should not be connected to any supply voltages, have any I/Os biased or receive any clocks. Upon exposure to "free air" (that is, unsealed packaging or a device removed from packaging material) the processor must be handled in accordance with moisture sensitivity labeling (MSL) as indicated on the packaging material.
TAC	Thermal Averaging Constant.
TAP	Test Access Point
TDP	Thermal Design Power.
V_{AXG}	Graphics core power supply.
V_{CC}	Processor core power supply.
V_{CCIO}	High Frequency I/O logic power supply
V_{CCPLL}	PLL power supply
V_{CCSA}	System Agent (memory controller, DMI, PCIe controllers, and display engine) power supply
V_{DDQ}	DDR3 power supply.
VLD	Variable Length Decoding.
V_{SS}	Processor ground.
x1	Refers to a Link or Port with one Physical Lane.
x16	Refers to a Link or Port with sixteen Physical Lanes.
x4	Refers to a Link or Port with four Physical Lanes.
x8	Refers to a Link or Port with eight Physical Lanes.

1.7 Related Documents

Refer to Table 1-3 for additional information.

Table 1-3. Related Documents

Document	Document Number/ Location
2nd Generation Intel® Core™ Processor Family Desktop, Intel® Pentium® Processor Family Desktop, and Intel® Celeron® Processor Family Desktop Datasheet, Volume 2	http://download.intel.com/design/processor/datashts/324642.pdf
2nd Generation Intel® Core™ Processor Family Desktop, Intel® Pentium® Processor Family Desktop, and Intel® Celeron® Processor Family Desktop Specification Update	http://download.intel.com/design/processor/specupdt/324643.pdf
2nd Generation Intel® Core™ Processor Family Desktop, Intel® Pentium® Processor Family Desktop, and Intel® Celeron® Processor Family Desktop, and LGA1155 Socket Thermal Mechanical Specifications and Design Guidelines	http://download.intel.com/design/processor/designex/324644.pdf
Intel® 6 Series Chipset and Intel® C200 Series Chipset Datasheet	www.intel.com/Assets/PDF/datasheet/324645.pdf
Intel® 6 Series Chipset and Intel® C200 Series Chipset Thermal Mechanical Specifications and Design Guidelines	www.intel.com/Assets/PDF/designguide/324647.pdf
Advanced Configuration and Power Interface Specification 3.0	http://www.acpi.info/
PCI Local Bus Specification 3.0	http://www.pcisig.com/specifications
Intel® TXT Measured Launched Environment Developer's Guide	http://www.intel.com/technology/security
Intel® 64 Architecture x2APIC Specification	http://www.intel.com/products/processor/manuals/
PCI Express Base Specification 2.0*	http://www.pcisig.com
DDR3 SDRAM Specification	http://www.jedec.org
DisplayPort Specification*	http://www.vesa.org
Intel® 64 and IA-32 Architectures Software Developer's Manuals	http://www.intel.com/products/processor/manuals/index.htm
Volume 1: Basic Architecture	253665
Volume 2A: Instruction Set Reference, A-M	253666
Volume 2B: Instruction Set Reference, N-Z	253667
Volume 3A: System Programming Guide	253668
Volume 3B: System Programming Guide	253669

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2 Interfaces

This chapter describes the interfaces supported by the processor.

2.1 System Memory Interface

2.1.1 System Memory Technology Supported

The Integrated Memory Controller (IMC) supports DDR3 protocols with two independent, 64-bit wide channels each accessing one or two DIMMs. The type of memory supported by the processor is dependant on the PCH SKU in the target platform. Refer to Chapter 1 for supported memory configuration details.

It supports a maximum of two DDR3 DIMMs per-channel; thus, allowing up to four device ranks per-channel.

- DDR3 Data Transfer Rates
  - 1066 MT/s (PC3-8500), 1333 MT/s (PC3-10600)
- DDR3 SO-DIMM Modules
  - Raw Card A – Dual Ranked x16 unbuffered non-ECC
  - Raw Card B – Single Ranked x8 unbuffered non-ECC
  - Raw Card C – Single Ranked x16 unbuffered non-ECC
  - Raw Card F – Dual Ranked x8 (planar) unbuffered non-ECC
- Desktop PCH platform DDR3 DIMM Modules
  - Raw Card A – Single Ranked x8 unbuffered non-ECC
  - Raw Card B – Dual Ranked x8 unbuffered non-ECC
  - Raw Card C – Single Ranked x16 unbuffered non-ECC
- Advanced Server/Workstation PCH platforms DDR3 DIMM Modules:
  - Raw Card A – Single Ranked x8 unbuffered non-ECC
  - Raw Card B – Dual Ranked x8 unbuffered non-ECC
  - Raw Card C – Single Ranked x16 unbuffered non-ECC
  - Raw Card D – Single Ranked x8 unbuffered ECC
  - Raw Card E – Dual Ranked x8 unbuffered ECC
- Essential/Standard Server PCH platforms DDR3 DIMM Modules:
  - Raw Card D – Single Ranked x8 unbuffered ECC
  - Raw Card E – Dual Ranked x8 unbuffered ECC

DDR3 DRAM Device Technology: 1-Gb, 2-Gb, and 4 Gb DDR3 DRAM Device technologies and addressing are supported.

Table 2-1. Supported UDIMM Module Configurations

Raw Card Version	DIMM Capacity	DRAM Device Technology	DRAM Organization	# of DRAM Devices	# of Physical Device Ranks	# of Row/Col Address Bits	# of Banks Inside DRAM	Page Size
Unbuffered/Non-ECC Supported DIMM Module Configurations								
A	1 GB	1 Gb	128 M X 8	8	2	14/10	8	8 K
	2 GB	2 Gb	128 M X 16	8	2	14/10	8	16 K
B	2 GB	1 Gb	128 M X 8	16	2	14/10	8	8 K
	4 GB	2 Gb	256 M X 8	16	2	15/10	8	8 K
	8 GB	4 Gb	512 M X 8	16	2	16/10	8	8 K
C	512 MB	1 Gb	64 M X 16	4	1	13/10	8	16 K
	1 GB	2 Gb	128 M X 16	4	1	14/10	8	16 K

Note: DIMM module support is based on availability and is subject to change.

Table 2-2. Supported SO-DIMM Module Configurations (AIO Only)[1,2]

Raw Card Version	DIMM Capacity	DRAM Device Technology	DRAM Organization	# of DRAM Devices	# of Physical Device Ranks	# of Row/Col Address Bits	# of Banks Inside DRAM	Page Size
A	1 GB	1 Gb	64 M x 16	8	2	13/10	8	8K
	2 GB	2 Gb	128 M x 16	8	2	14/10	8	8K
B	1 GB	1 Gb	128 M x 8	8	1	14/10	8	8K
	2 GB	2 Gb	256 M x 8	8	1	15/10	8	8K
C	512 MB	1 Gb	64 M x 16	4	1	13/10	8	8K
	1 GB	2 Gb	128 M x 16	4	1	14/10	8	8K
F	2 GB	1 Gb	128 M x 8	16	2	14/10	8	8K
	4 GB	2 Gb	256 M x 8	16	2	15/10	8	8K
	8 GB	4 Gb	512 M x 8	16	2	16/ 10	8	8K

Notes:
1. System memory configurations are based on availability and are subject to change.
2. Interface does not support ULV/LV memory modules or ULV/LV DIMMs.

2.1.2 System Memory Timing Support

The IMC supports the following DDR3 Speed Bin, CAS Write Latency (CWL), and command signal mode timings on the main memory interface:

- t_{CL} = CAS Latency
- t_{RCD} = Activate Command to READ or WRITE Command delay
- t_{RP} = PRECHARGE Command Period
- CWL = CAS Write Latency
- Command Signal modes = 1n indicates a new command may be issued every clock and 2n indicates a new command may be issued every 2 clocks. Command launch mode programming depends on the transfer rate and memory configuration.

Table 2-3. DDR3 System Memory Timing Support

Segment	Transfer Rate (MT/s)	tCL (tCK)	tRCD (tCK)	tRP (tCK)	CWL (tCK)	DPC	CMD Mode	Notes[1]
All Desktop segments	1066	7	7	7	6	1	1n/2n	
						2	2n	
		8	8	8	6	1	1n/2n	
						2	2n	
	1333	9	9	9	7	1	1n/2n	
						2	2n	

Notes:

1. System memory timing support is based on availability and is subject to change.

2.1.3 System Memory Organization Modes

The IMC supports two memory organization modes—single-channel and dual-channel. Depending upon how the DIMM Modules are populated in each memory channel, a number of different configurations can exist.

2.1.3.1 Single-Channel Mode

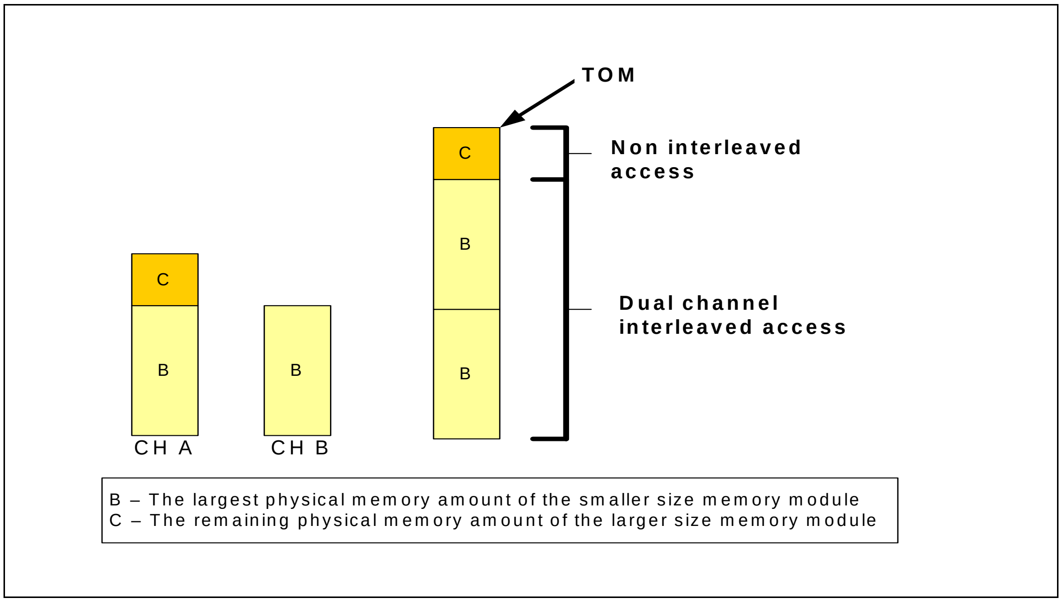
In this mode, all memory cycles are directed to a single-channel. Single-channel mode is used when either Channel A or Channel B DIMM connectors are populated in any order, but not both.

2.1.3.2 Dual-Channel Mode – Intel® Flex Memory Technology Mode

The IMC supports Intel Flex Memory Technology Mode. Memory is divided into a symmetric and an asymmetric zone. The symmetric zone starts at the lowest address in each channel and is contiguous until the asymmetric zone begins or until the top address of the channel with the smaller capacity is reached. In this mode, the system runs with one zone of dual-channel mode and one zone of single-channel mode, simultaneously, across the whole memory array.

Note: Channels A and B can be mapped for physical channels 0 and 1 respectively or vice versa; however, channel A size must be greater or equal to channel B size.

Figure 2-1. Intel® Flex Memory Technology Operation



2.1.3.2.1 Dual-Channel Symmetric Mode

Dual-Channel Symmetric mode, also known as interleaved mode, provides maximum performance on real world applications. Addresses are ping-ponged between the channels after each cache line (64-byte boundary). If there are two requests, and the second request is to an address on the opposite channel from the first, that request can be sent before data from the first request has returned. If two consecutive cache lines are requested, both may be retrieved simultaneously since they are ensured to be on opposite channels. Use Dual-Channel Symmetric mode when both Channel A and Channel B DIMM connectors are populated in any order, with the total amount of memory in each channel being the same.

When both channels are populated with the same memory capacity and the boundary between the dual channel zone and the single channel zone is the top of memory, IMC operates completely in Dual-Channel Symmetric mode.

Note: The DRAM device technology and width may vary from one channel to the other.

2.1.4 Rules for Populating Memory Slots

In all modes, the frequency of system memory is the lowest frequency of all memory modules placed in the system, as determined through the SPD registers on the memory modules. The system memory controller supports one or two DIMM connectors per channel. The usage of DIMM modules with different latencies is allowed, but in that case, the worst latency (per channel) will be used. For dual-channel modes, both channels must have a DIMM connector populated and for single-channel mode, only a single-channel may have one or both DIMM connectors populated.

Note: In a 2 DIMM Per Channel (2DPC) daisy chain layout memory configuration, the furthest DIMM from the processor of any given channel must always be populated first.

2.1.5 Technology Enhancements of Intel® Fast Memory Access (Intel® FMA)

The following sections describe the Just-in-Time Scheduling, Command Overlap, and Out-of-Order Scheduling Intel FMA technology enhancements.

2.1.5.1 Just-in-Time Command Scheduling

The memory controller has an advanced command scheduler where all pending requests are examined simultaneously to determine the most efficient request to be issued next. The most efficient request is picked from all pending requests and issued to system memory Just-in-Time to make optimal use of Command Overlapping. Thus, instead of having all memory access requests go individually through an arbitration mechanism forcing requests to be executed one at a time, they can be started without interfering with the current request allowing for concurrent issuing of requests. This allows for optimized bandwidth and reduced latency while maintaining appropriate command spacing to meet system memory protocol.

2.1.5.2 Command Overlap

Command Overlap allows the insertion of the DRAM commands between the Activate, Precharge, and Read/Write commands normally used, as long as the inserted commands do not affect the currently executing command. Multiple commands can be issued in an overlapping manner, increasing the efficiency of system memory protocol.

2.1.5.3 Out-of-Order Scheduling

While leveraging the Just-in-Time Scheduling and Command Overlap enhancements, the IMC continuously monitors pending requests to system memory for the best use of bandwidth and reduction of latency. If there are multiple requests to the same open page, these requests would be launched in a back to back manner to make optimum use of the open memory page. This ability to reorder requests on the fly allows the IMC to further reduce latency and increase bandwidth efficiency.

2.1.6 Memory Type Range Registers (MTRRs) Enhancement

The processor has 2 additional MTRRs (total 10 MTRRs). These additional MTRRs are specially important in supporting larger system memory beyond 4 GB.

2.1.7 Data Scrambling

The memory controller incorporates a DDR3 Data Scrambling feature to minimize the impact of excessive di/dt on the platform DDR3 VRs due to successive 1s and 0s on the data bus. Past experience has demonstrated that traffic on the data bus is not random and can have energy concentrated at specific spectral harmonics creating high di/dt that is generally limited by data patterns that excite resonance between the package inductance and on-die capacitances. As a result, the memory controller uses a data scrambling feature to create pseudo-random patterns on the DDR3 data bus to reduce the impact of any excessive di/dt.

2.2 PCI Express* Interface

This section describes the PCI Express interface capabilities of the processor. See the *PCI Express Base Specification* for details of PCI Express.

The number of PCI Express controllers is dependent on the platform. Refer to Chapter 1 for details.

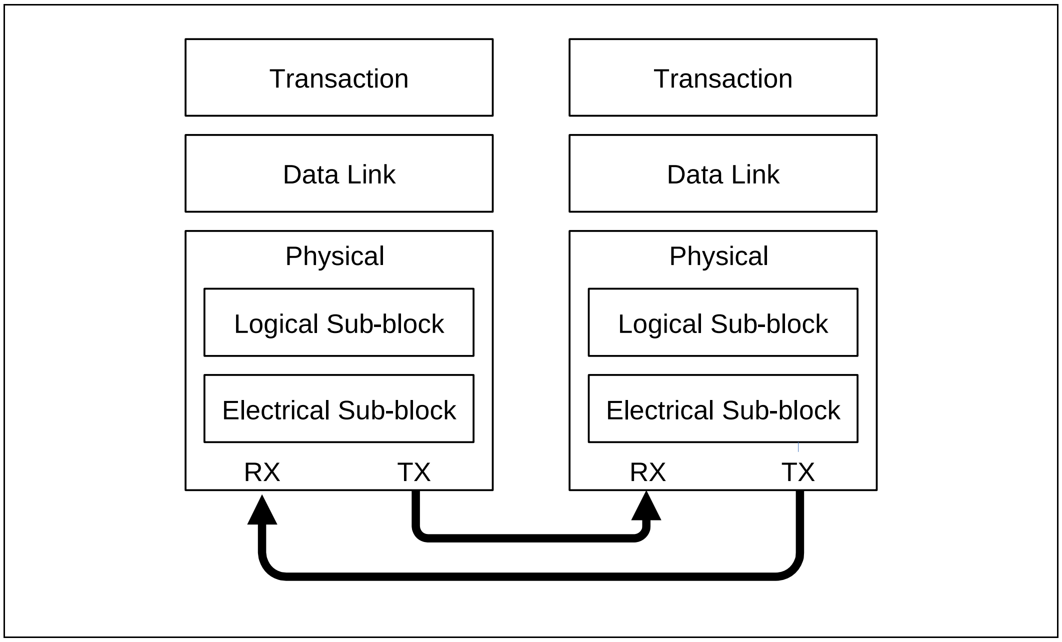
2.2.1 PCI Express* Architecture

Compatibility with the PCI addressing model is maintained to ensure that all existing applications and drivers operate unchanged.

The PCI Express configuration uses standard mechanisms as defined in the PCI Plug-and-Play specification. The initial recovered clock speed of 1.25 GHz results in 2.5 Gb/s/direction that provides a 250 MB/s communications channel in each direction (500 MB/s total). That is close to twice the data rate of classic PCI. The fact that 8b/10b encoding is used accounts for the 250 MB/s where quick calculations would imply 300 MB/s. The external graphics ports support Gen2 speed as well. At 5.0 GT/s, Gen 2 operation results in twice as much bandwidth per lane as compared to Gen 1 operation. When operating with two PCIe controllers, each controller can be operating at either 2.5 GT/s or 5.0 GT/s.

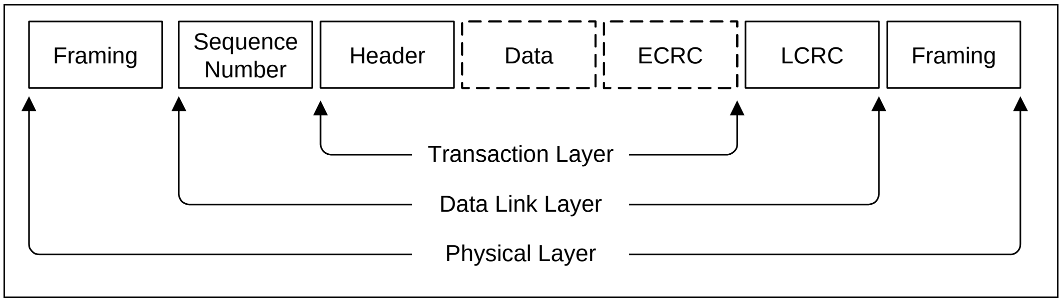
The PCI Express architecture is specified in three layers—Transaction Layer, Data Link Layer, and Physical Layer. The partitioning in the component is not necessarily along these same boundaries. Refer to Figure 2-2 for the PCI Express Layering Diagram.

Figure 2-2. PCI Express* Layering Diagram



PCI Express uses packets to communicate information between components. Packets are formed in the Transaction and Data Link Layers to carry the information from the transmitting component to the receiving component. As the transmitted packets flow through the other layers, they are extended with additional information necessary to handle packets at those layers. At the receiving side, the reverse process occurs and packets get transformed from their Physical Layer representation to the Data Link Layer representation and finally (for Transaction Layer Packets) to the form that can be processed by the Transaction Layer of the receiving device.

Figure 2-3. Packet Flow through the Layers



2.2.1.1 Transaction Layer

The upper layer of the PCI Express architecture is the Transaction Layer. The Transaction Layer's primary responsibility is the assembly and disassembly of Transaction Layer Packets (TLPs). TLPs are used to communicate transactions, such as read and write, as well as certain types of events. The Transaction Layer also manages flow control of TLPs.

2.2.1.2 Data Link Layer

The middle layer in the PCI Express stack, the Data Link Layer, serves as an intermediate stage between the Transaction Layer and the Physical Layer. Responsibilities of Data Link Layer include link management, error detection, and error correction.

The transmission side of the Data Link Layer accepts TLPs assembled by the Transaction Layer, calculates and applies data protection code and TLP sequence number, and submits them to Physical Layer for transmission across the Link. The receiving Data Link Layer is responsible for checking the integrity of received TLPs and for submitting them to the Transaction Layer for further processing. On detection of TLP error(s), this layer is responsible for requesting retransmission of TLPs until information is correctly received, or the Link is determined to have failed. The Data Link Layer also generates and consumes packets that are used for Link management functions.

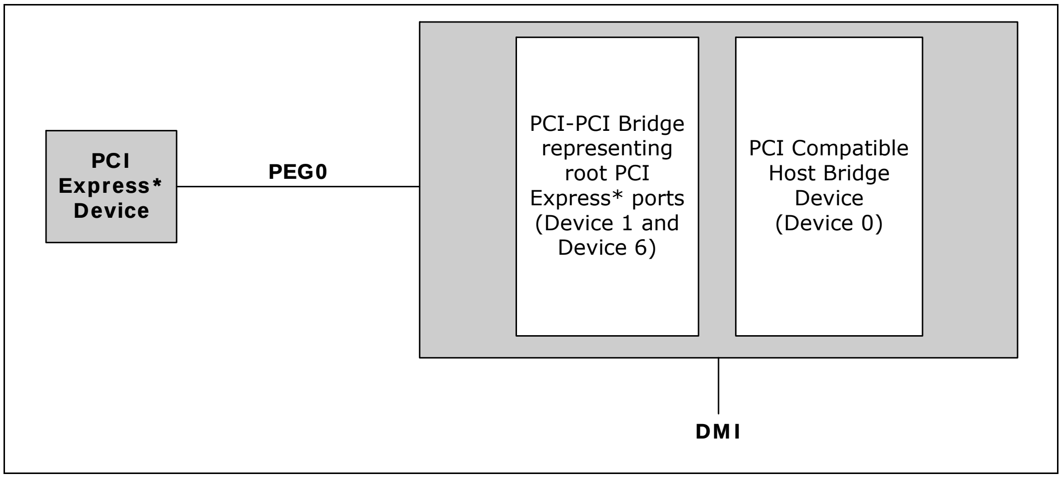
2.2.1.3 Physical Layer

The Physical Layer includes all circuitry for interface operation, including driver and input buffers, parallel-to-serial and serial-to-parallel conversion, PLL(s), and impedance matching circuitry. It also includes logical functions related to interface initialization and maintenance. The Physical Layer exchanges data with the Data Link Layer in an implementation-specific format, and is responsible for converting this to an appropriate serialized format and transmitting it across the PCI Express Link at a frequency and width compatible with the remote device.

2.2.2 PCI Express* Configuration Mechanism

The PCI Express (external graphics) link is mapped through a PCI-to-PCI bridge structure.

Figure 2-4. PCI Express* Related Register Structures in the Processor



PCI Express extends the configuration space to 4096 bytes per-device/function, as compared to 256 bytes allowed by the Conventional PCI Specification. PCI Express configuration space is divided into a PCI-compatible region (that consists of the first 256 bytes of a logical device's configuration space) and an extended PCI Express region (that consists of the remaining configuration space). The PCI-compatible region can be accessed using either the mechanisms defined in the PCI specification or using the enhanced PCI Express configuration access mechanism described in the PCI Express Enhanced Configuration Mechanism section.

The PCI Express Host Bridge is required to translate the memory-mapped PCI Express configuration space accesses from the host processor to PCI Express configuration cycles. To maintain compatibility with PCI configuration addressing mechanisms, it is recommended that system software access the enhanced configuration space using 32-bit operations (32-bit aligned) only. See the *PCI Express Base Specification* for details of both the PCI-compatible and PCI Express Enhanced configuration mechanisms and transaction rules.

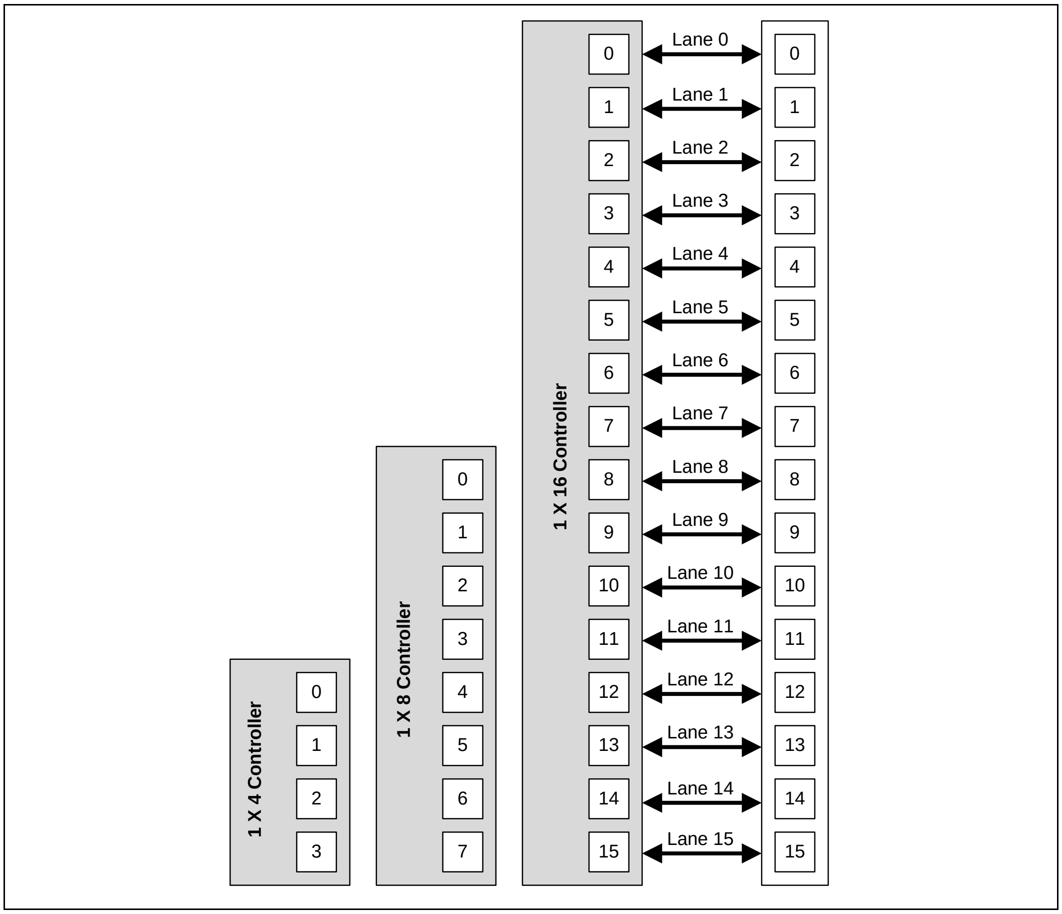
2.2.3 PCI Express* Port

The PCI Express interface on the processor is a single, 16-lane (x16) port that can also be configured at narrower widths. The PCI Express port is compliant with the *PCI Express Base Specification, Revision 2.0.*

2.2.4 PCI Express* Lanes Connection

Figure 2-5 demonstrates the PCIe lanes mapping.

Figure 2-5. PCI Express* Typical Operation 16 lanes Mapping



2.3 Direct Media Interface (DMI)

Direct Media Interface (DMI) connects the processor and the PCH. Next generation DMI2 is supported.

Note: Only DMI x4 configuration is supported.

2.3.1 DMI Error Flow

DMI can only generate SERR in response to errors, never SCI, SMI, MSI, PCI INT, or GPE. Any DMI related SERR activity is associated with Device 0.

2.3.2 Processor / PCH Compatibility Assumptions

The processor is compatible with the Intel® 6 Series Chipset PCH. The processor is not compatible with any previous PCH products.

2.3.3 DMI Link Down

The DMI link going down is a fatal, unrecoverable error. If the DMI data link goes to data link down, after the link was up, then the DMI link hangs the system by not allowing the link to retrain to prevent data corruption. This link behavior is controlled by the PCH.

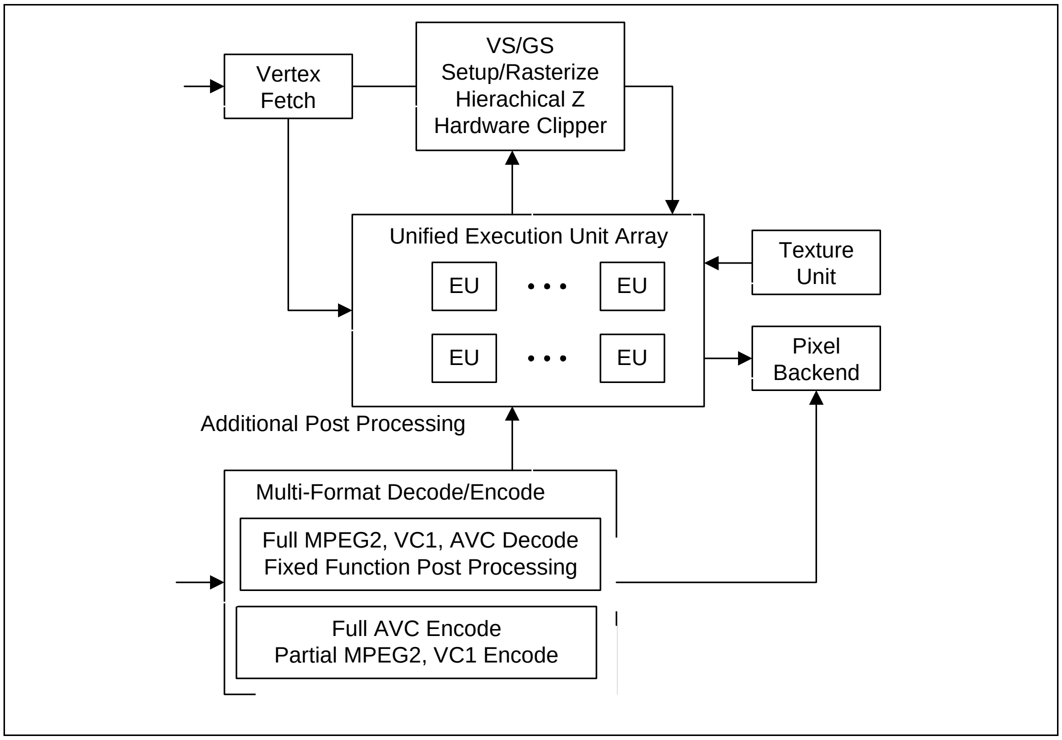
Downstream transactions that had been successfully transmitted across the link prior to the link going down may be processed as normal. No completions from downstream, non-posted transactions are returned upstream over the DMI link after a link down event.

2.4 Processor Graphics Controller (GT)

New Graphics Engine Architecture includes 3D compute elements, Multi-format hardware-assisted decode/encode Pipeline, and Mid-Level Cache (MLC) for superior high definition playback, video quality, and improved 3D performance and Media.

Display Engine in the Uncore handles delivering the pixels to the screen. GSA (Graphics in System Agent) is the primary Channel interface for display memory accesses and "PCI-like" traffic in and out.

Figure 2-6. Processor Graphics Controller Unit Block Diagram



2.4.1 3D and Video Engines for Graphics Processing

The 3D graphics pipeline architecture simultaneously operates on different primitives or on different portions of the same primitive. All the cores are fully programmable, increasing the versatility of the 3D Engine. The Gen 6.0 3D engine provides the following performance and power-management enhancements:

- Up to 12 Execution units (EUs)
- Hierarchal-Z
- Video quality enhancements

2.4.1.1 3D Engine Execution Units

- Supports up to 12 EUs. The EUs perform 128-bit wide execution per clock.
- Support SIMD8 instructions for vertex processing and SIMD16 instructions for pixel processing.

2.4.1.2 3D Pipeline

2.4.1.2.1 Vertex Fetch (VF) Stage

The VF stage executes 3DPRIMITIVE commands. Some enhancements have been included to better support legacy D3D APIs as well as SGI OpenGL*.

2.4.1.2.2 Vertex Shader (VS) Stage

The VS stage performs shading of vertices output by the VF function. The VS unit produces an output vertex reference for every input vertex reference received from the VF unit, in the order received.

2.4.1.2.3 Geometry Shader (GS) Stage

The GS stage receives inputs from the VS stage. Compiled application-provided GS programs, specifying an algorithm to convert the vertices of an input object into some output primitives. For example, a GS shader may convert lines of a line strip into polygons representing a corresponding segment of a blade of grass centered on the line. Or it could use adjacency information to detect silhouette edges of triangles and output polygons extruding out from the edges.

2.4.1.2.4 Clip Stage

The Clip stage performs general processing on incoming 3D objects. However, it also includes specialized logic to perform a Clip Test function on incoming objects. The Clip Test optimizes generalized 3D Clipping. The Clip unit examines the position of incoming vertices, and accepts/rejects 3D objects based on its Clip algorithm.

2.4.1.2.5 Strips and Fans (SF) Stage

The SF stage performs setup operations required to rasterize 3D objects. The outputs from the SF stage to the Windower stage contain implementation-specific information required for the rasterization of objects and also supports clipping of primitives to some extent.

2.4.1.2.6 Windower/IZ (WIZ) Stage

The WIZ unit performs an early depth test, which removes failing pixels and eliminates unnecessary processing overhead.

The Windower uses the parameters provided by the SF unit in the object-specific rasterization algorithms. The WIZ unit rasterizes objects into the corresponding set of pixels. The Windower is also capable of performing dithering, whereby the illusion of a higher resolution when using low-bpp channels in color buffers is possible. Color dithering diffuses the sharp color bands seen on smooth-shaded objects.

2.4.1.3 Video Engine

The Video Engine handles the non-3D (media/video) applications. It includes support for VLD and MPEG2 decode in hardware.

2.4.1.4 2D Engine

The 2D Engine contains BLT (Block Level Transfer) functionality and an extensive set of 2D instructions. To take advantage of the 3D during engine's functionality, some BLT functions make use of the 3D renderer.

2.4.1.4.1 Processor Graphics VGA Registers

The 2D registers consists of original VGA registers and others to support graphics modes that have color depths, resolutions, and hardware acceleration features that go beyond the original VGA standard.

2.4.1.4.2 Logical 128-Bit Fixed BLT and 256 Fill Engine

This BLT engine accelerates the GUI of Microsoft Windows* operating systems. The 128-bit BLT engine provides hardware acceleration of block transfers of pixel data for many common Windows operations. The BLT engine can be used for the following:

- Move rectangular blocks of data between memory locations
- Data alignment
- To perform logical operations (raster ops)

The rectangular block of data does not change, as it is transferred between memory locations. The allowable memory transfers are between: cacheable system memory and frame buffer memory, frame buffer memory and frame buffer memory, and within system memory. Data to be transferred can consist of regions of memory, patterns, or solid color fills. A pattern is always 8 x 8 pixels wide and may be 8, 16, or 32 bits per pixel.

The BLT engine expands monochrome data into a color depth of 8, 16, or 32 bits. BLTs can be either opaque or transparent. Opaque transfers move the data specified to the destination. Transparent transfers compare destination color to source color and write according to the mode of transparency selected.

Data is horizontally and vertically aligned at the destination. If the destination for the BLT overlaps with the source memory location, the BLT engine specifies which area in memory to begin the BLT transfer. Hardware is included for all 256 raster operations (source, pattern, and destination) defined by Microsoft, including transparent BLT.

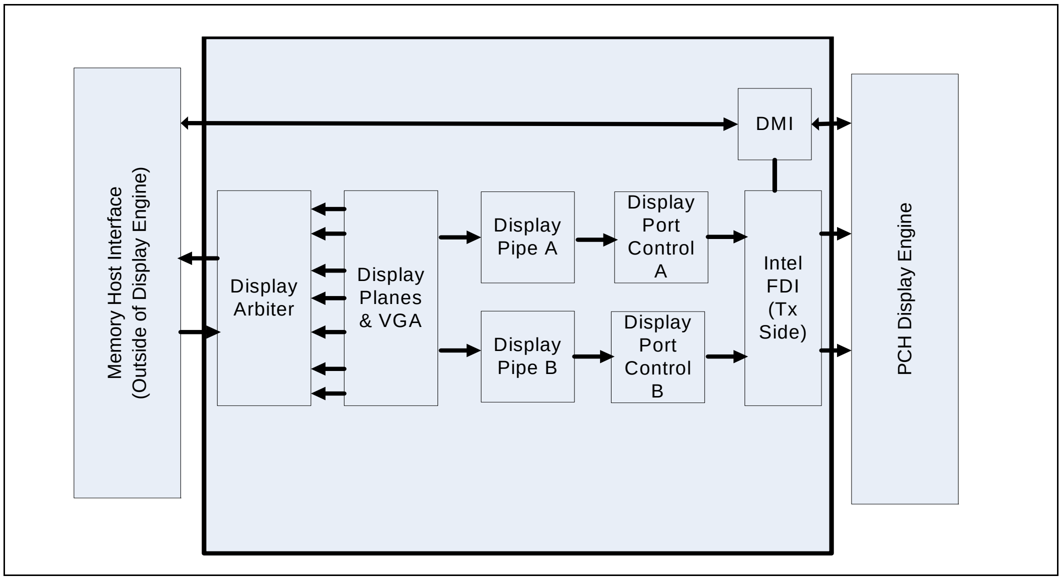
The BLT engine has instructions to invoke BLT and stretch BLT operations, permitting software to set up instruction buffers and use batch processing. The BLT engine can perform hardware clipping during BLTs.

2.4.2 Processor Graphics Display

The Processor Graphics controller display pipe can be broken down into three components:

- Display Planes
- Display Pipes
- DisplayPort and Intel FDI

Figure 2-7. Processor Display Block Diagram



2.4.2.1 Display Planes

A display plane is a single displayed surface in memory and contains one image (desktop, cursor, overlay). It is the portion of the display hardware logic that defines the format and location of a rectangular region of memory that can be displayed on display output device and delivers that data to a display pipe. This is clocked by the Core Display Clock.

2.4.2.1.1 Planes A and B

Planes A and B are the main display planes and are associated with Pipes A and B respectively. The two display pipes are independent, allowing for support of two independent display streams. They are both double-buffered, which minimizes latency and improves visual quality.

2.4.2.1.2 Sprite A and B

Sprite A and Sprite B are planes optimized for video decode, and are associated with Planes A and B respectively. Sprite A and B are also double-buffered.

2.4.2.1.3 Cursors A and B

Cursors A and B are small, fixed-sized planes dedicated for mouse cursor acceleration, and are associated with Planes A and B respectively. These planes support resolutions up to 256 x 256 each.

2.4.2.1.4 Video Graphics Array (VGA)

VGA is used for boot, safe mode, legacy games, etc. It can be changed by an application without OS/driver notification, due to legacy requirements.

2.4.2.2 Display Pipes

The display pipe blends and synchronizes pixel data received from one or more display planes and adds the timing of the display output device upon which the image is displayed. This is clocked by the Display Reference clock inputs.

The display pipes A and B operate independently of each other at the rate of 1 pixel per clock. They can attach to any of the display ports. Each pipe sends display data to the PCH over the Intel Flexible Display Interface (Intel FDI).

2.4.2.3 Display Ports

The display ports consist of output logic and pins that transmit the display data to the associated encoding logic and send the data to the display device (that is, LVDS, HDMI*, DVI, SDVO, and so on). All display interfaces connecting external displays are now repartitioned and driven from the PCH.

2.4.3 Intel® Flexible Display Interface (Intel® FDI)

The Intel Flexible Display Interface (Intel® FDI) is a proprietary link for carrying display traffic from the Processor Graphics controller to the PCH display I/Os. Intel® FDI supports two independent channels—one for pipe A and one for pipe B.

- Each channel has four transmit (Tx) differential pairs used for transporting pixel and framing data from the display engine.
- Each channel has one single-ended LineSync and one FrameSync input (1-V CMOS signaling).
- One display interrupt line input (1-V CMOS signaling).
- Intel® FDI may dynamically scalable down to 2X or 1X based on actual display bandwidth requirements.
- Common 100-MHz reference clock.
- Each channel transports at a rate of 2.7 Gbps.
- PCH supports end-to-end lane reversal across both channels (no reversal support required in the processor).

2.4.4 Multi-Graphics Controller Multi-Monitor Support

The processor supports simultaneous use of the Processor Graphics Controller (GT) and a x16 PCI Express Graphics (PEG) device.

The processor supports a maximum of 2 displays connected to the PEG card in parallel with up to 2 displays connected to the PCH.

Note: When supporting Multi Graphics controllers Multi-Monitors, “drag and drop” between monitors and the 2x8 PEG is not supported.

2.5 Platform Environment Control Interface (PECI)

The PECI is a one-wire interface that provides a communication channel between a PECI client (processor) and a PECI master. The processor implements a PECI interface to:

- Allow communication of processor thermal and other information to the PECI master.
- Read averaged Digital Thermal Sensor (DTS) values for fan speed control.

2.6 Interface Clocking

2.6.1 Internal Clocking Requirements

Table 2-4. Reference Clock

Reference Input Clock	Input Frequency	Associated PLL
BCLK[0]/BCLK#[0]	100 MHz	Processor/Memory/Graphics/PCIe/DMI/FDI

§ §

3 Technologies

This chapter provides a high-level description of Intel technologies implemented in the processor.

The implementation of the features may vary between the processor SKUs.

Details on the different technologies of Intel processors and other relevant external notes are located at the Intel technology web site: http://www.intel.com/technology/

3.1 Intel® Virtualization Technology (Intel® VT)

Intel Virtualization Technology (Intel® VT) makes a single system appear as multiple independent systems to software. This allows multiple, independent operating systems to run simultaneously on a single system. Intel VT comprises technology components to support virtualization of platforms based on Intel architecture microprocessors and chipsets. Intel Virtualization Technology (Intel VT-x) added hardware support in the processor to improve the virtualization performance and robustness. Intel Virtualization Technology for Directed I/O (Intel VT-d) adds chipset hardware implementation to support and improve I/O virtualization performance and robustness.

Intel VT-x specifications and functional descriptions are included in the *Intel® 64 and IA-32 Architectures Software Developer's Manual*, *Volume 3B* and is available at:

http://www.intel.com/products/processor/manuals/index.htm

The Intel VT-d specification and other VT documents can be referenced at:

http://www.intel.com/technology/virtualization/index.htm

3.1.1 Intel® Virtualization Technology (Intel® VT) for IA-32, Intel® 64 and Intel® Architecture (Intel® VT-x) Objectives

Intel VT-x provides hardware acceleration for virtualization of IA platforms. Virtual Machine Monitor (VMM) can use Intel VT-x features to provide improved a reliable virtualized platform. By using Intel VT-x, a VMM is:

- **Robust:** VMMs no longer need to use paravirtualization or binary translation. This means that they will be able to run off-the-shelf OSs and applications without any special steps.
- **Enhanced:** Intel VT enables VMMs to run 64-bit guest operating systems on IA x86 processors.
- **More reliable:** Due to the hardware support, VMMs can now be smaller, less complex, and more efficient. This improves reliability and availability and reduces the potential for software conflicts.
- **More secure:** The use of hardware transitions in the VMM strengthens the isolation of VMs and further prevents corruption of one VM from affecting others on the same system.

3.1.2 Intel® Virtualization Technology (Intel® VT) for IA-32, Intel® 64 and Intel® Architecture (Intel® VT-x) Features

The processor core supports the following Intel VT-x features:

- Extended Page Tables (EPT)
    - EPT is hardware assisted page table virtualization
    - It eliminates VM exits from guest OS to the VMM for shadow page-table maintenance
- Virtual Processor IDs (VPID)
    - Ability to assign a VM ID to tag processor core hardware structures (such as TLBs)
    - This avoids flushes on VM transitions to give a lower-cost VM transition time and an overall reduction in virtualization overhead.
- Guest Preemption Timer
    - Mechanism for a VMM to preempt the execution of a guest OS after an amount of time specified by the VMM. The VMM sets a timer value before entering a guest
    - The feature aids VMM developers in flexibility and Quality of Service (QoS) assurances
- Descriptor-Table Exiting
    - Descriptor-table exiting allows a VMM to protect a guest OS from internal (malicious software based) attack by preventing relocation of key system data structures like IDT (interrupt descriptor table), GDT (global descriptor table), LDT (local descriptor table), and TSS (task segment selector).
    - A VMM using this feature can intercept (by a VM exit) attempts to relocate these data structures and prevent them from being tampered by malicious software.

3.1.3 Intel® Virtualization Technology (Intel® VT) for Directed I/O (Intel® VT-d) Objectives

The key Intel VT-d objectives are domain-based isolation and hardware-based virtualization. A domain can be abstractly defined as an isolated environment in a platform to which a subset of host physical memory is allocated. Virtualization allows for the creation of one or more partitions on a single system. This could be multiple partitions in the same operating system, or there can be multiple operating system instances running on the same system – offering benefits such as system consolidation, legacy migration, activity partitioning, or security.

3.1.4 Intel® Virtualization Technology (Intel® VT) for Directed I/O (Intel® VT-d) Features

The processor supports the following Intel VT-d features:

- Memory controller and Processor Graphics comply with Intel® VT-d 1.2 specification.
- Two VT-d DMA remap engines.
  - iGraphics DMA remap engine
  - DMI/PEG
- Support for root entry, context entry, and default context
- 39-bit guest physical address and host physical address widths
- Support for 4K page sizes only
- Support for register-based fault recording only (for single entry only) and support for MSI interrupts for faults
- Support for both leaf and non-leaf caching
- Support for boot protection of default page table
- Support for non-caching of invalid page table entries
- Support for hardware based flushing of translated but pending writes and pending reads, on IOTLB invalidation
- Support for page-selective IOTLB invalidation
- MSI cycles (MemWr to address FEEx_xxxxh) not translated
  - Translation faults result in cycle forwarding to VBIOS region (byte enables masked for writes). Returned data may be bogus for internal agents, PEG/DMI interfaces return unsupported request status
- Interrupt Remapping is supported
- Queued invalidation is supported.
- VT-d translation bypass address range is supported (Pass Through)

Note: Intel VT-d Technology may not be available on all SKUs.

3.1.5 Intel® Virtualization Technology (Intel® VT) for Directed I/O (Intel® VT-d) Features Not Supported

The following features are not supported by the processor with Intel VT-d:

- No support for PCISIG endpoint caching (ATS)
- No support for Intel VT-d read prefetching/snarfing (that is, translations within a cacheline are not stored in an internal buffer for reuse for subsequent translations).
- No support for advance fault reporting
- No support for super pages
- No support for Intel VT-d translation bypass address range (such usage models need to be resolved with VMM help in setting up the page tables correctly)

3.2 Intel® Trusted Execution Technology (Intel® TXT)

Intel Trusted Execution Technology (Intel TXT) defines platform-level enhancements that provide the building blocks for creating trusted platforms.

The Intel TXT platform helps to provide the authenticity of the controlling environment such that those wishing to rely on the platform can make an appropriate trust decision. The Intel TXT platform determines the identity of the controlling environment by accurately measuring and verifying the controlling software.

Another aspect of the trust decision is the ability of the platform to resist attempts to change the controlling environment. The Intel TXT platform will resist attempts by software processes to change the controlling environment or bypass the bounds set by the controlling environment.

Intel TXT is a set of extensions designed to provide a measured and controlled launch of system software that will then establish a protected environment for itself and any additional software that it may execute.

These extensions enhance two areas:

- The launching of the Measured Launched Environment (MLE)
- The protection of the MLE from potential corruption

The enhanced platform provides these launch and control interfaces using Safer Mode Extensions (SMX).

The SMX interface includes the following functions:

- Measured/Verified launch of the MLE
- Mechanisms to ensure the above measurement is protected and stored in a secure location
- Protection mechanisms that allow the MLE to control attempts to modify itself

For more information, refer to the *Intel® TXT Measured Launched Environment Developer's Guide* in http://www.intel.com/technology/security.

3.3 Intel® Hyper-Threading Technology (Intel® HT Technology)

The processor supports Intel® Hyper-Threading Technology (Intel® HT Technology), that allows an execution core to function as two logical processors. While some execution resources (such as caches, execution units, and buses) are shared, each logical processor has its own architectural state with its own set of general-purpose registers and control registers. This feature must be enabled using the BIOS and requires operating system support.

Intel recommends enabling Intel HT Technology with Microsoft Windows 7*, Microsoft Windows Vista*, Microsoft Windows* XP Professional/Windows* XP Home, and disabling Intel HT Technology using the BIOS for all previous versions of Windows operating systems. For more information on Intel HT Technology, see http://www.intel.com/technology/platform-technology/hyper-threading/.

3.4 Intel® Turbo Boost Technology

Intel® Turbo Boost Technology is a feature that allows the processor core to opportunistically and automatically run faster than its rated operating frequency/render clock if it is operating below power, temperature, and current limits. The Intel Turbo Boost Technology feature is designed to increase performance of both multi-threaded and single-threaded workloads. Maximum frequency is dependant on the SKU and number of active cores. No special hardware support is necessary for Intel Turbo Boost Technology. BIOS and the OS can enable or disable Intel Turbo Boost Technology. Compared with previous generation products, Intel Turbo Boost Technology will increase the ratio of application power to TDP. Thus, thermal solutions and platform cooling that are designed to less than thermal design guidance might experience thermal and performance issues since more applications will tend to run at the maximum power limit for significant periods of time.

Note: Intel Turbo Boost Technology may not be available on all SKUs.

3.4.1 Intel® Turbo Boost Technology Frequency

The processor's rated frequency assumes that all execution cores are running an application at the thermal design power (TDP). However, under typical operation, not all cores are active. Therefore, most applications are consuming less than the TDP at the rated frequency. To take advantage of the available thermal headroom, the active cores can increase their operating frequency.

To determine the highest performance frequency amongst active cores, the processor takes the following into consideration:

- The number of cores operating in the C0 state.
- The estimated current consumption.
- The estimated power consumption.
- The temperature.

Any of these factors can affect the maximum frequency for a given workload. If the power, current, or thermal limit is reached, the processor will automatically reduce the frequency to stay with its TDP limit.

Note: Intel Turbo Boost Technology processor frequencies are only active if the operating system is requesting the P0 state. For more information on P-states and C-states, refer to Chapter 4, "Power Management".

3.4.2 Intel® Turbo Boost Technology Graphics Frequency

Graphics render frequency is selected by the processor dynamically based on graphics workload demand. The processor can optimize both processor and Processor Graphics performance by managing power for the overall package. For the Processor Graphics, this allows an increase in the render core frequency and increased graphics performance for graphics intensive workloads. In addition, during processor intensive workloads when the graphics power is low, the processor core can increase its frequency higher within the package power limit. Enabling Intel Turbo Boost Technology will maximize the performance of the processor core and the graphics render frequency within the specified package power levels.

3.5 Intel® Advanced Vector Extensions (Intel® AVX)

Intel Advanced Vector Extensions (Intel AVX) is the latest expansion of the Intel instruction set. It extends the Intel Streaming SIMD Extensions (Intel SSE) from 128-bit vectors into 256-bit vectors. Intel AVX addresses the continued need for vector floating-point performance in mainstream scientific and engineering numerical applications, visual processing, recognition, data-mining/synthesis, gaming, physics, cryptography and other areas of applications. The enhancement in Intel AVX allows for improved performance due to wider vectors, new extensible syntax, and rich functionality including the ability to better manage, rearrange, and sort data. For more information on Intel AVX, see http://www.intel.com/software/avx

3.6 Intel® Advanced Encryption Standard New Instructions (Intel® AES-NI)

The processor supports Advanced Encryption Standard New Instructions (Intel AES-NI) that are a set of Single Instruction Multiple Data (SIMD) instructions that enable fast and secure data encryption and decryption based on the Advanced Encryption Standard (AES). Intel AES-NI are valuable for a wide range of cryptographic applications; such as, applications that perform bulk encryption/decryption, authentication, random number generation, and authenticated encryption. AES is broadly accepted as the standard for both government and industry applications, and is widely deployed in various protocols.

Intel AES-NI consists of six Intel SSE instructions. Four instructions, AESENC, AESENCLAST, AESDEC, and AESDELAST facilitate high performance AES encryption and decryption. The other two, AESIMC and AESKEYGENASSIST, support the AES key expansion procedure. Together, these instructions provide a full hardware for supporting AES, offering security, high performance, and a great deal of flexibility.

3.6.1 PCLMULQDQ Instruction

The processor supports the carry-less multiplication instruction, PCLMULQDQ. PCLMULQDQ is a Single Instruction Multiple Data (SIMD) instruction that computes the 128-bit carry-less multiplication of two, 64-bit operands without generating and propagating carries. Carry-less multiplication is an essential processing component of several cryptographic systems and standards. Hence, accelerating carry-less multiplication can significantly contribute to achieving high speed secure computing and communication.

3.7 Intel® 64 Architecture x2APIC

The x2APIC architecture extends the xAPIC architecture that provides a key mechanism for interrupt delivery. This extension is intended primarily to increase processor addressability.

Specifically, x2APIC:

- Retains all key elements of compatibility to the xAPIC architecture
    - delivery modes
    - interrupt and processor priorities
    - interrupt sources
    - interrupt destination types

- Provides extensions to scale processor addressability for both the logical and physical destination modes
- Adds new features to enhance performance of interrupt delivery
- Reduces complexity of logical destination mode interrupt delivery on link based architectures

The key enhancements provided by the x2APIC architecture over xAPIC are the following:

- Support for two modes of operation to provide backward compatibility and extensibility for future platform innovations
    - In xAPIC compatibility mode, APIC registers are accessed through a memory mapped interface to a 4 KB page, identical to the xAPIC architecture.
    - In x2APIC mode, APIC registers are accessed through Model Specific Register (MSR) interfaces. In this mode, the x2APIC architecture provides significantly increased processor addressability and some enhancements on interrupt delivery.
- Increased range of processor addressability in x2APIC mode
    - Physical xAPIC ID field increases from 8 bits to 32 bits, allowing for interrupt processor addressability up to 4G-1 processors in physical destination mode. A processor implementation of x2APIC architecture can support fewer than 32-bits in a software transparent fashion.
    - Logical xAPIC ID field increases from 8 bits to 32 bits. The 32-bit logical x2APIC ID is partitioned into two sub-fields—a 16-bit cluster ID and a 16-bit logical ID within the cluster. Consequently, ((2^20) -16) processors can be addressed in logical destination mode. Processor implementations can support fewer than 16 bits in the cluster ID sub-field and logical ID sub-field in a software agnostic fashion.
- More efficient MSR interface to access APIC registers
    - To enhance inter-processor and self directed interrupt delivery as well as the ability to virtualize the local APIC, the APIC register set can be accessed only through MSR based interfaces in the x2APIC mode. The Memory Mapped IO (MMIO) interface used by xAPIC is not supported in the x2APIC mode.
- The semantics for accessing APIC registers have been revised to simplify the programming of frequently-used APIC registers by system software. Specifically, the software semantics for using the Interrupt Command Register (ICR) and End Of Interrupt (EOI) registers have been modified to allow for more efficient delivery and dispatching of interrupts.

The x2APIC extensions are made available to system software by enabling the local x2APIC unit in the “x2APIC” mode. To benefit from x2APIC capabilities, a new Operating System and a new BIOS are both needed, with special support for the x2APIC mode.

The x2APIC architecture provides backward compatibility to the xAPIC architecture and forward extendibility for future Intel platform innovations.

Note: Intel x2APIC technology may not be available on all processor SKUs.

For more information, refer to the *Intel® 64 Architecture x2APIC Specification* at http://www.intel.com/products/processor/manuals/

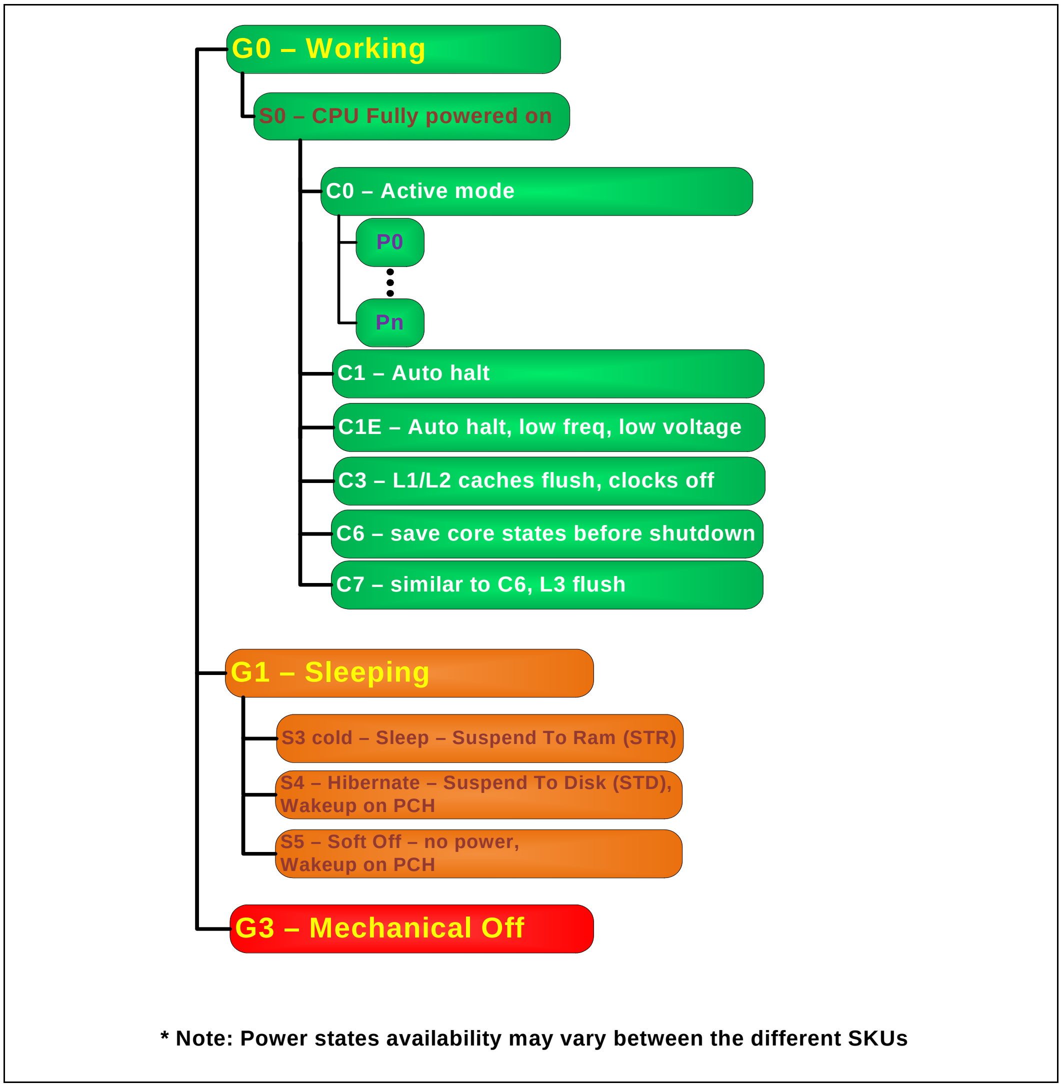
§ §

4 Power Management

This chapter provides information on the following power management topics:

- Advanced Configuration and Power Interface (ACPI) States
- Processor Core
- Integrated Memory Controller (IMC)
- PCI Express*
- Direct Media Interface (DMI)
- Processor Graphics Controller

Figure 4-1. Power States



*** Note: Power states availability may vary between the different SKUs**

4.1 Advanced Configuration and Power Interface (ACPI) States Supported

The ACPI states supported by the processor are described in this section.

4.1.1 System States

Table 4-1. System States

State	Description
G0/S0	Full On
G1/S3-Cold	Suspend-to-RAM (STR). Context saved to memory (S3-Hot is not supported by the processor).
G1/S4	Suspend-to-Disk (STD). All power lost (except wakeup on PCH).
G2/S5	Soft off. All power lost (except wakeup on PCH). Total reboot.
G3	Mechanical off. All power removed from system.

4.1.2 Processor Core / Package Idle States

Table 4-2. Processor Core / Package State Support

State	Description
C0	Active mode, processor executing code
C1	AutoHALT state
C1E	AutoHALT state with lowest frequency and voltage operating point
C3	Execution cores in C3 flush their L1 instruction cache, L1 data cache, and L2 cache to the L3 shared cache. Clocks are shut off to each core.
C6	Execution cores in this state save their architectural state before removing core voltage.

4.1.3 Integrated Memory Controller States

Table 4-3. Integrated Memory Controller States

State	Description
Power up	CKE asserted. Active mode
Pre-charge Power-down	CKE de-asserted (not self-refresh) with all banks closed
Active Power-Down	CKE de-asserted (not self-refresh) with minimum one bank active
Self-Refresh	CKE de-asserted using device self-refresh

4.1.4 PCI Express* Link States

Table 4-4. PCI Express* Link States

State	Description
L0	Full on – Active transfer state
L0s	First Active Power Management low power state – Low exit latency
L1	Lowest Active Power Management – Longer exit latency
L3	Lowest power state (power-off) – Longest exit latency

4.1.5 Direct Media Interface (DMI) States

Table 4-5. Direct Media Interface (DMI) States

State	Description
L0	Full on – Active transfer state
L0s	First Active Power Management low power state – Low exit latency
L1	Lowest Active Power Management – Longer exit latency
L3	Lowest power state (power-off) – Longest exit latency

4.1.6 Processor Graphics Controller States

Table 4-6. Processor Graphics Controller States

State	Description
D0	Full on, display active
D3 Cold	Power-off

4.1.7 Interface State Combinations

Table 4-7. G, S, and C State Combinations

Global (G) State	Sleep (S) State	Processor Package (C) State	Processor State	System Clocks	Description
G0	S0	C0	Full On	On	Full On
G0	S0	C1/C1E	Auto-Halt	On	Auto-Halt
G0	S0	C3	Deep Sleep	On	Deep Sleep
G0	S0	C6	Deep Power-down	On	Deep Power-down
G1	S3	Power off		Off, except RTC	Suspend to RAM
G1	S4	Power off		Off, except RTC	Suspend to Disk
G2	S5	Power off		Off, except RTC	Soft Off
G3	NA	Power off		Power off	Hard off

4.2 Processor Core Power Management

While executing code, Enhanced Intel SpeedStep Technology optimizes the processor’s frequency and core voltage based on workload. Each frequency and voltage operating point is defined by ACPI as a P-state. When the processor is not executing code, it is idle. A low-power idle state is defined by ACPI as a C-state. In general, lower power C-states have longer entry and exit latencies.

4.2.1 Enhanced Intel® SpeedStep® Technology

The following are the key features of Enhanced Intel SpeedStep Technology:

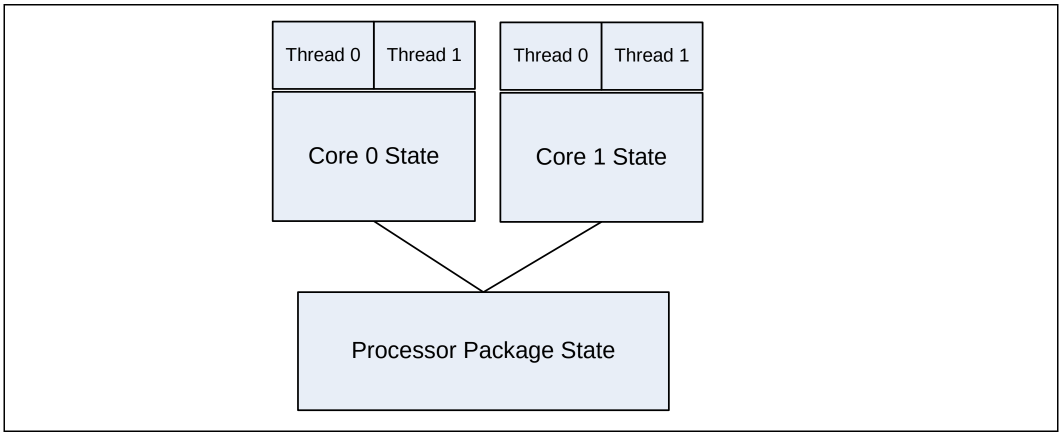
- Multiple frequency and voltage points for optimal performance and power efficiency. These operating points are known as P-states.
- Frequency selection is software controlled by writing to processor MSRs. The voltage is optimized based on the selected frequency and the number of active processor cores.
  - If the target frequency is higher than the current frequency, V_{CC} is ramped up in steps to an optimized voltage. This voltage is signaled by the SVID bus to the voltage regulator. Once the voltage is established, the PLL locks on to the target frequency.
  - If the target frequency is lower than the current frequency, the PLL locks to the target frequency, then transitions to a lower voltage by signaling the target voltage on SVID bus.
  - All active processor cores share the same frequency and voltage. In a multi-core processor, the highest frequency P-state requested amongst all active cores is selected.
  - Software-requested transitions are accepted at any time. If a previous transition is in progress, the new transition is deferred until the previous transition is completed.
- The processor controls voltage ramp rates internally to ensure glitch-free transitions.
- Because there is low transition latency between P-states, a significant number of transitions per-second are possible.

4.2.2 Low-Power Idle States

When the processor is idle, low-power idle states (C-states) are used to save power. More power savings actions are taken for numerically higher C-states. However, higher C-states have longer exit and entry latencies. Resolution of C-states occur at the thread, processor core, and processor package level. Thread-level C-states are available if Intel HT Technology is enabled.

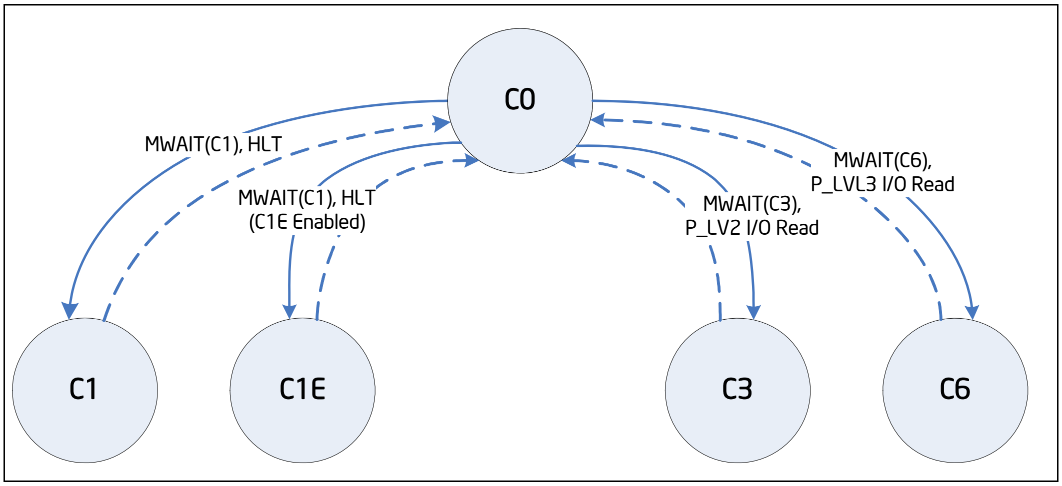
Caution: Long term reliability cannot be assured unless all the Low Power Idle States are enabled.

Figure 4-2. Idle Power Management Breakdown of the Processor Cores



Entry and exit of the C-States at the thread and core level are shown in Figure 4-3.

Figure 4-3. Thread and Core C-State Entry and Exit



While individual threads can request low power C-states, power saving actions only take place once the core C-state is resolved. Core C-states are automatically resolved by the processor. For thread and core C-states, a transition to and from C0 is required before entering any other C-state.

Table 4-8. Coordination of Thread Power States at the Core Level

Processor Core C-State		Thread 1			
		C0	C1	C3	C6
Thread 0	C0	C0	C0	C0	C0
	C1	C0	C1[1]	C1[1]	C1[1]
	C3	C0	C1[1]	C3	C3
	C6	C0	C1[1]	C3	C6

Note:

1. If enabled, the core C-state will be C1E if all enabled cores have also resolved a core C1 state or higher.

4.2.3 Requesting Low-Power Idle States

The primary software interfaces for requesting low power idle states are through the MWAIT instruction with sub-state hints and the HLT instruction (for C1 and C1E). However, software may make C-state requests using the legacy method of I/O reads from the ACPI-defined processor clock control registers, referred to as P_LVLx. This method of requesting C-states provides legacy support for operating systems that initiate C-state transitions using I/O reads.

For legacy operating systems, P_LVLx I/O reads are converted within the processor to the equivalent MWAIT C-state request. Therefore, P_LVLx reads do not directly result in I/O reads to the system. The feature, known as I/O MWAIT redirection, must be enabled in the BIOS.

Note: The P_LVLx I/O Monitor address needs to be set up before using the P_LVLx I/O read interface. Each P-LVLx is mapped to the supported MWAIT(Cx) instruction as shown in Table 4-9.

Table 4-9. P_LVLx to MWAIT Conversion

P_LVLx	MWAIT(Cx)	Notes
P_LVL2	MWAIT(C3)	
P_LVL3	MWAIT(C6)	C6. No sub-states allowed.

The BIOS can write to the C-state range field of the PMG_IO_CAPTURE MSR to restrict the range of I/O addresses that are trapped and emulate MWAIT like functionality. Any P_LVLx reads outside of this range does not cause an I/O redirection to MWAIT(Cx) like request. They fall through like a normal I/O instruction.

Note: When P_LVLx I/O instructions are used, MWAIT substates cannot be defined. The MWAIT substate is always zero if I/O MWAIT redirection is used. By default, P_LVLx I/O redirections enable the MWAIT 'break on EFLAGS.IF’ feature that triggers a wakeup on an interrupt, even if interrupts are masked by EFLAGS.IF.

4.2.4 Core C-states

The following are general rules for all core C-states, unless specified otherwise:

- A core C-State is determined by the lowest numerical thread state (such as Thread 0 requests C1E while Thread 1 requests C3, resulting in a core C1E state). See Table 4-7.
- A core transitions to C0 state when:
  - An interrupt occurs
  - There is an access to the monitored address if the state was entered using an MWAIT instruction
- For core C1/C1E, core C3, and core C6, an interrupt directed toward a single thread wakes only that thread. However, since both threads are no longer at the same core C-state, the core resolves to C0.
- A system reset re-initializes all processor cores.

4.2.4.1 Core C0 State

The normal operating state of a core where code is being executed.

4.2.4.2 Core C1/C1E State

C1/C1E is a low power state entered when all threads within a core execute a HLT or MWAIT(C1/C1E) instruction.

A System Management Interrupt (SMI) handler returns execution to either Normal state or the C1/C1E state. See the *Intel® 64 and IA-32 Architecture Software Developer's Manual, Volume 3A/3B: System Programmer's Guide for more information.*

While a core is in C1/C1E state, it processes bus snoops and snoops from other threads. For more information on C1E, see Section 4.2.5.2.

4.2.4.3 Core C3 State

Individual threads of a core can enter the C3 state by initiating a P_LVL2 I/O read to the P_BLK or an MWAIT(C3) instruction. A core in C3 state flushes the contents of its L1 instruction cache, L1 data cache, and L2 cache to the shared L3 cache, while maintaining its architectural state. All core clocks are stopped at this point. Because the core's caches are flushed, the processor does not wake any core that is in the C3 state when either a snoop is detected or when another core accesses cacheable memory.

4.2.4.4 Core C6 State

Individual threads of a core can enter the C6 state by initiating a P_LVL3 I/O read or an MWAIT(C6) instruction. Before entering core C6, the core will save its architectural state to a dedicated SRAM. Once complete, a core will have its voltage reduced to zero volts. During exit, the core is powered on and its architectural state is restored.

4.2.4.5 C-State Auto-Demotion

In general, deeper C-states such as C6 have long latencies and have higher energy entry/exit costs. The resulting performance and energy penalties become significant when the entry/exit frequency of a deeper C-state is high. Therefore, incorrect or inefficient usage of deeper C-states have a negative impact on power. To increase residency and improve power in deeper C-states, the processor supports C-state auto-demotion.

There are two C-State auto-demotion options:

- C6 to C3
- C6/C3 To C1

The decision to demote a core from C6 to C3 or C3/C6 to C1 is based on each core's immediate residency history. Upon each core C6 request, the core C-state is demoted to C3 or C1 until a sufficient amount of residency has been established. At that point, a core is allowed to go into C3/C6. Each option can be run concurrently or individually.

This feature is disabled by default. BIOS must enable it in the PMG_CST_CONFIG_CONTROL register. The auto-demotion policy is also configured by this register.

4.2.5 Package C-States

The processor supports C0, C1/C1E, C3, and C6 power states. The following is a summary of the general rules for package C-state entry. These apply to all package C-states unless specified otherwise:

- A package C-state request is determined by the lowest numerical core C-state amongst all cores.
- A package C-state is automatically resolved by the processor depending on the core idle power states and the status of the platform components.
  - Each core can be at a lower idle power state than the package if the platform does not grant the processor permission to enter a requested package C-state.
  - The platform may allow additional power savings to be realized in the processor.
  - For package C-states, the processor is not required to enter C0 before entering any other C-state.

The processor exits a package C-state when a break event is detected. Depending on the type of break event, the processor does the following:

- If a core break event is received, the target core is activated and the break event message is forwarded to the target core.
  - If the break event is not masked, the target core enters the core C0 state and the processor enters package C0.
- If the break event was due to a memory access or snoop request.
  - But the platform did not request to keep the processor in a higher package C-state, the package returns to its previous C-state.
  - And the platform requests a higher power C-state, the memory access or snoop request is serviced and the package remains in the higher power C-state.

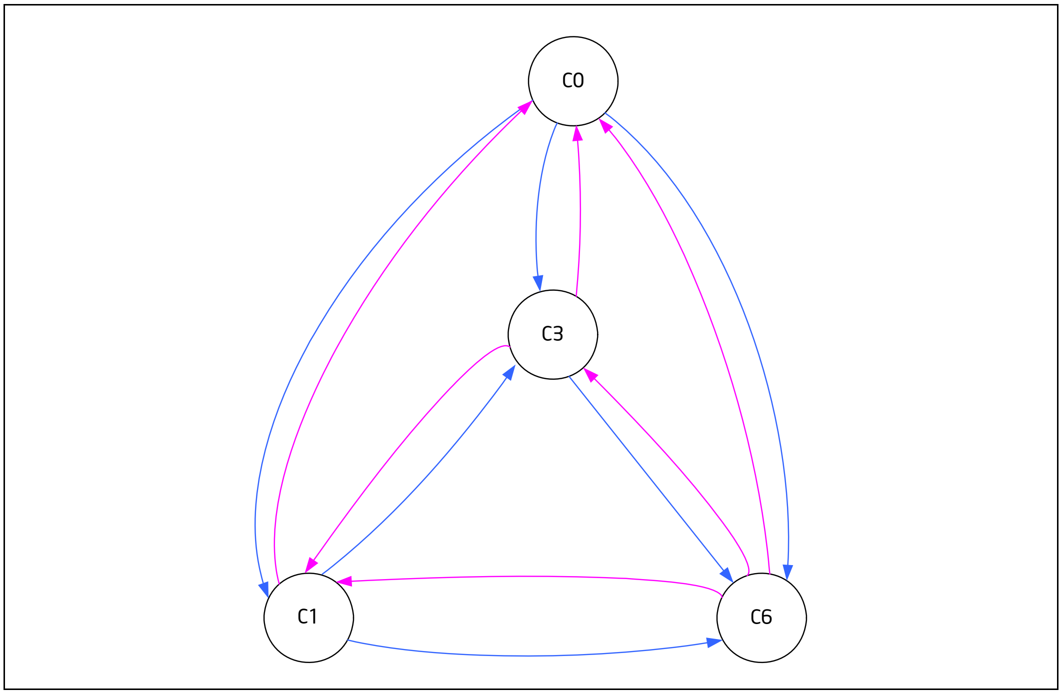
Table 4-10. Coordination of Core Power States at the Package Level

Package C-State		**Core 1**			
		C0	**C1**	**C3**	**C6**
Core 0	**C0**	C0	C0	C0	C0
	C1	C0	C1[1]	C1[1]	C1[1]
	C3	C0	C1[1]	C3	C3
	C6	C0	C1[1]	C3	C6

Note:

1. If enabled, the package C-state will be C1E if all cores have resolved a core C1 state or higher.

Figure 4-4. Package C-State Entry and Exit



4.2.5.1 Package C0

This is the normal operating state for the processor. The processor remains in the normal state when at least one of its cores is in the C0 or C1 state or when the platform has not granted permission to the processor to go into a low power state. Individual cores may be in lower power idle states while the package is in C0.

4.2.5.2 Package C1/C1E

No additional power reduction actions are taken in the package C1 state. However, if the C1E sub-state is enabled, the processor automatically transitions to the lowest supported core clock frequency, followed by a reduction in voltage.

The package enters the C1 low power state when:

- At least one core is in the C1 state.
- The other cores are in a C1 or lower power state.

The package enters the C1E state when:

- All cores have directly requested C1E using MWAIT(C1) with a C1E sub-state hint.
- All cores are in a power state lower that C1/C1E but the package low power state is limited to C1/C1E using the PMG_CST_CONFIG_CONTROL MSR.
- All cores have requested C1 using HLT or MWAIT(C1) and C1E auto-promotion is enabled in IA32_MISC_ENABLES.

No notification to the system occurs upon entry to C1/C1E.

4.2.5.3 Package C3 State

A processor enters the package C3 low power state when:

- At least one core is in the C3 state.
- The other cores are in a C3 or lower power state, and the processor has been granted permission by the platform.
- The platform has not granted a request to a package C6 state but has allowed a package C6 state.

In package C3-state, the L3 shared cache is valid.

4.2.5.4 Package C6 State

A processor enters the package C6 low power state when:

- At least one core is in the C6 state.
- The other cores are in a C6 or lower power state, and the processor has been granted permission by the platform.

In package C6 state, all cores have saved their architectural state and have had their core voltages reduced to zero volts. The L3 shared cache is still powered and snoopable in this state. The processor remains in package C6 state as long as any part of the L3 cache is active.

4.3 Integrated Memory Controller (IMC) Power Management

The main memory is power managed during normal operation and in low-power ACPI Cx states.

4.3.1 Disabling Unused System Memory Outputs

Any system memory (SM) interface signal that goes to a memory module connector in which it is not connected to any actual memory devices (such as DIMM connector is unpopulated, or is single-sided) is tri-stated. The benefits of disabling unused SM signals are:

- Reduced power consumption.
- Reduced possible overshoot/undershoot signal quality issues seen by the processor I/O buffer receivers caused by reflections from potentially un-terminated transmission lines.

When a given rank is not populated, the corresponding chip select and CKE signals are not driven.

At reset, all rows must be assumed to be populated, until it can be proven that they are not populated. This is due to the fact that when CKE is tristated with an DIMM present, the DIMM is not ensured to maintain data integrity.

SCKE tri-state should be enabled by BIOS where appropriate, since at reset all rows must be assumed to be populated.

4.3.2 DRAM Power Management and Initialization

The processor implements extensive support for power management on the SDRAM interface. There are four SDRAM operations associated with the Clock Enable (CKE) signals that the SDRAM controller supports. The processor drives four CKE pins to perform these operations.

The CKE is one of the power-save means. When CKE is off the internal DDR clock is disabled and the DDR power is reduced. The power-saving differs according the selected mode and the DDR type used. For more information, please refer to the IDD table in the DDR specification.

The DDR specification defines 3 levels of power-down that differ in power-saving and in wakeup time:

1. **Active power-down (APD):** This mode is entered if there are open pages when de-asserting CKE. In this mode the open pages are retained. Power-saving in this mode is the lowest. Power consumption of DDR is defined by IDD3P. Exiting this mode is fined by tXP – small number of cycles.
2. **Precharged power-down (PPD):** This mode is entered if all banks in DDR are precharged when de-asserting CKE. Power-saving in this mode is intermediate – better than APD, but less than DLL-off. Power consumption is defined by IDD2P1. Exiting this mode is defined by tXP. Difference from APD mode is that when waking-up all page-buffers are empty
3. **DLL-off:** In this mode the data-in DLLs on DDR are off. Power-saving in this mode is the best among all power-modes. Power consumption is defined by IDD2P1. Exiting this mode is defined by tXP, but also tXPDLL (10 – 20 according to DDR type) cycles until first data transfer is allowed.

The processor supports 5 different types of power-down. The different modes are the power-down modes supported by DDR3 and combinations of these. The type of CKE power-down is defined by the configuration. The are options are:

1. No power-down
2. APD: The rank enters power-down as soon as idle-timer expires, no matter what is the bank status
3. PPD: When idle timer expires the MC sends PRE-all to rank and then enters power-down
4. DLL-off: same as option (2) but DDR is configured to DLL-off
5. APD, change to PPD (APD-PPD): Begins as option (1), and when all page-close timers of the rank are expired, it wakes the rank, issues PRE-all, and returns to PPD APD, change to DLL-off (APD_DLLoff) – Begins as option (1), and when all page-close timers of the rank are expired, it wakes the rank, issues PRE-all and returns to DLL-off power-down

The CKE is determined per rank when it is inactive. Each rank has an idle-counter. The idle-counter starts counting as soon as the rank has no accesses, and if it expires, the rank may enter power-down while no new transactions to the rank arrive to queues. The idle-counter begins counting at the last incoming transaction arrival.

It is important to understand that since the power-down decision is per rank, the MC can find many opportunities to power-down ranks even while running memory intensive applications, and savings are significant (may be a few watts, according to the DDR specification). This is significant when each channel is populated with more ranks.

Selection of power modes should be according to power-performance or thermal trade-offs of a given system:

- When trying to achieve maximum performance and power or thermal consideration is not an issue: use no power-down.
- In a system that tries to minimize power-consumption, try to use the deepest power-down mode possible – DLL-off or APD_DLLoff.
- In high-performance systems with dense packaging (that is, complex thermal design) the power-down mode should be considered in order to reduce the heating and avoid DDR throttling caused by the heating.

Control of the power-mode through CRB-BIOS: The BIOS selects by default no-power-down. There are knobs to change the power-down selected mode.

Another control is the idle timer expiration count. This is set through PM_PDWN_config bits 7:0 (MCHBAR +4CB0). As this timer is set to a shorter time, the MC will have more opportunities to put DDR in power-down. The minimum recommended value for this register is 15. There is no BIOS hook to set this register. Customers who choose to change the value of this register can do it by changing the BIOS. For experiments, this register can be modified in real time if BIOS did not lock the MC registers.

Note: In APD, APD-PPD, and APD-DLLoff there is no point in setting the idle-counter in the same range of page-close idle timer.

Another option associated with CKE power-down is the S_DLL-off. When this option is enabled, the SBR I/O slave DLLs go off when all channel ranks are in power-down. (Do **not** confuse it with the DLL-off mode, in which the **DDR** DLLs are off). This mode requires to define the I/O slave DLL wakeup time.

4.3.2.1 Initialization Role of CKE

During power-up, CKE is the only input to the SDRAM that has its level recognized (other than the DDR3 reset pin) once power is applied. It must be driven LOW by the DDR controller to make sure the SDRAM components float DQ and DQS during power-up. CKE signals remain LOW (while any reset is active) until the BIOS writes to a configuration register. Using this method, CKE is ensured to remain inactive for much longer than the specified 200 micro-seconds after power and clocks to SDRAM devices are stable.

4.3.2.2 Conditional Self-Refresh

Intel Rapid Memory Power Management (Intel RMPM) conditionally places memory into self-refresh in the package C3 and C6 low-power states. Intel RMPM functionality depends on the graphics/display state (relevant only when processor graphics is being used), as well as memory traffic patterns generated by other connected I/O devices. The target behavior is to enter self-refresh as long as there are no memory requests to service.

When entering the S3 – Suspend-to-RAM (STR) state or S0 conditional self-refresh, the processor core flushes pending cycles and then enters all SDRAM ranks into self-refresh. The CKE signals remain LOW so the SDRAM devices perform self-refresh.

4.3.2.3 Dynamic Power-down Operation

Dynamic power-down of memory is employed during normal operation. Based on idle conditions, a given memory rank may be powered down. The IMC implements aggressive CKE control to dynamically put the DRAM devices in a power-down state. The processor core controller can be configured to put the devices in *active power-down* (CKE de-assertion with open pages) or *precharge power-down* (CKE de-assertion with all pages closed). Precharge power-down provides greater power savings but has a bigger performance impact, since all pages will first be closed before putting the devices in power-down mode.

If dynamic power-down is enabled, all ranks are powered up before doing a refresh cycle and all ranks are powered down at the end of refresh.

4.3.2.4 DRAM I/O Power Management

Unused signals should be disabled to save power and reduce electromagnetic interference. This includes all signals associated with an unused memory channel. Clocks can be controlled on a per SO-DIMM basis. Exceptions are made for per SO-DIMM control signals such as CS#, CKE, and ODT for unpopulated SO-DIMM slots.

The I/O buffer for an unused signal should be tri-stated (output driver disabled), the input receiver (differential sense-amp) should be disabled, and any DLL circuitry related ONLY to unused signals should be disabled. The input path must be gated to prevent spurious results due to noise on the unused signals (typically handled automatically when input receiver is disabled).

4.4 PCI Express* Power Management

- Active power management support using L0s, and L1 states.
- All inputs and outputs disabled in L2/L3 Ready state.

Note: PEG interface does not support Hot Plug.

Note: Power impact may be observed when PEG link disable power management state is used.

4.5 Direct Media Interface (DMI) Power Management

- Active power management support using L0s/L1 state.

4.6 Graphics Power Management

4.6.1 Intel® Rapid Memory Power Management (Intel® RMPM) (also known as CxSR)

The Intel Rapid Memory Power Management puts rows of memory into self refresh mode during C3/C6 to allow the system to remain in the lower power states longer. Desktop processors routinely save power during runtime conditions by entering the C3, C6 state. Intel RMPM is an indirect method of power saving that can have a significant effect on the system as a whole.

4.6.2 Intel® Graphics Performance Modulation Technology (Intel® GPMT)

Intel Graphics Power Modulation Technology (Intel GPMT) is a method for saving power in the graphics adapter while continuing to display and process data in the adapter. This method will switch the render frequency and/or render voltage dynamically between higher and lower power states supported on the platform based on render engine workload.

In products where Intel® Graphics Dynamic Frequency (also known as Turbo Boost Technology) is supported and enabled, the functionality of Intel GPMT will be maintained by Intel® Graphics Dynamic Frequency (also known as Turbo Boost Technology).

4.6.3 Graphics Render C-State

Render C-State (RC6) is a technique designed to optimize the average power to the graphics render engine during times of idleness of the render engine. Render C-state is entered when the graphics render engine, blitter engine and the video engine have no workload being currently worked on and no outstanding graphics memory transactions. When the idleness condition is met, the Integrated Graphics will program the VR into a low voltage state (~0.4 V) through the SVID bus.

4.6.4 Intel® Smart 2D Display Technology (Intel® S2DDT)

Intel S2DDT reduces display refresh memory traffic by reducing memory reads required for display refresh. Power consumption is reduced by less accesses to the IMC. S2DDT is only enabled in single pipe mode.

Intel S2DDT is most effective with:

- Display images well suited to compression, such as text windows, slide shows, and so on. Poor examples are 3D games.
- Static screens such as screens with significant portions of the background showing 2D applications, processor benchmarks, and so on, or conditions when the processor is idle. Poor examples are full-screen 3D games and benchmarks that flip the display image at or near display refresh rates.

4.6.5 Intel® Graphics Dynamic Frequency

Intel® Graphics Dynamic Frequency Technology is the ability of the processor and graphics cores to opportunistically increase frequency and/or voltage above the ensured processor and graphics frequency for the given part. Intel® Graphics Dynamic Frequency Technology is a performance feature that makes use of unused package power and thermals to increase application performance. The increase in frequency is determined by how much power and thermal budget is available in the package, and the application demand for additional processor or graphics performance. The processor core control is maintained by an embedded controller. The graphics driver dynamically adjusts between P-States to maintain optimal performance, power, and thermals. The graphics driver will always place the graphics engine in its lowest possible P-State; thereby, acting in the same capacity as Intel GPMT.

4.7 Thermal Power Management

See Section 4.6 for all graphics thermal power management-related features.

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5 Thermal Management

For thermal specifications and design guidelines, refer to the *2nd Generation Intel® Core™ Processor Family Desktop, Intel® Pentium® Processor Family Desktop, and Intel® Celeron® Processor Family Desktop, and LGA1155 Socket Thermal and Mechanical Specifications and Design Guidelines*.

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6 Signal Description

This chapter describes the processor signals. They are arranged in functional groups according to their associated interface or category. The following notations are used to describe the signal type.

Notations	Signal Type
I	Input Pin
O	Output Pin
I/O	Bi-directional Input/Output Pin

The signal description also includes the type of buffer used for the particular signal (see Table 6-1).

Table 6-1. Signal Description Buffer Types

Signal	Description
PCI Express*	PCI Express interface signals. These signals are compatible with PCI Express* 2.0 Signalling Environment AC Specifications and are AC coupled. The buffers are not 3.3-V tolerant. Refer to the PCIe specification.
DMI	Direct Media Interface signals. These signals are based on PCI Express* 2.0 Signaling Environment AC Specifications (5 GT/s), but are DC coupled. The buffers are not 3.3-V tolerant.
CMOS	CMOS buffers. 1.1-V tolerant
DDR3	DDR3 buffers: 1.5-V tolerant
A	Analog reference or output. May be used as a threshold voltage or for buffer compensation
Ref	Voltage reference signal
Asynchronous[1]	Signal has no timing relationship with any reference clock.

Notes:
1. Qualifier for a buffer type.

6.1 System Memory Interface Signals

Table 6-2. Memory Channel A Signals

Signal Name	Description	Direction / Buffer Type
SA_BS[2:0]	**Bank Select:** These signals define which banks are selected within each SDRAM rank.	O DDR3
SA_WE#	**Write Enable Control Signal:** This signal is used with SA_RAS# and SA_CAS# (along with SA_CS#) to define the SDRAM Commands.	O DDR3
SA_RAS#	**RAS Control Signal:** This signal is used with SA_CAS# and SA_WE# (along with SA_CS#) to define the SRAM Commands.	O DDR3
SA_CAS#	**CAS Control Signal:** This signal is used with SA_RAS# and SA_WE# (along with SA_CS#) to define the SRAM Commands.	O DDR3
SA_DQS[8:0] SA_DQS#[8:0]	**Data Strobes:** SA_DQS[8:0] and its complement signal group make up a differential strobe pair. The data is captured at the crossing point of SA_DQS[8:0] and its SA_DQS#[8:0] during read and write transactions.	I/O DDR3
SA_DQ[63:0]	**Data Bus:** Channel A data signal interface to the SDRAM data bus.	I/O DDR3
SA_MA[15:0]	**Memory Address:** These signals are used to provide the multiplexed row and column address to the SDRAM.	O DDR3
SA_CK[3:0]	**SDRAM Differential Clock:** Channel A SDRAM Differential clock signal pair. The crossing of the positive edge of SA_CK and the negative edge of its complement SA_CK# are used to sample the command and control signals on the SDRAM.	O DDR3
SA_CK#[3:0]	**SDRAM Inverted Differential Clock:** Channel A SDRAM Differential clock signal-pair complement.	O DDR3
SA_CKE[3:0]	**Clock Enable:** (1 per rank). Used to: • Initialize the SDRAMs during power-up • Power-down SDRAM ranks • Place all SDRAM ranks into and out of self-refresh during STR	O DDR3
SA_CS#[3:0]	**Chip Select:** (1 per rank). Used to select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank.	O DDR3
SA_ODT[3:0]	**On Die Termination:** Active Termination Control.	O DDR3

Table 6-3. Memory Channel B Signals

Signal Name	Description	Direction / Buffer Type
SB_BS[2:0]	**Bank Select:** These signals define which banks are selected within each SDRAM rank.	O DDR3
SB_WE#	**Write Enable Control Signal:** This signal is used with SB_RAS# and SB_CAS# (along with SB_CS#) to define the SDRAM Commands.	O DDR3
SB_RAS#	**RAS Control Signal:** This signal is used with SB_CAS# and SB_WE# (along with SB_CS#) to define the SRAM Commands.	O DDR3
SB_CAS#	**CAS Control Signal:** This signal is used with SB_RAS# and SB_WE# (along with SB_CS#) to define the SRAM Commands.	O DDR3
SB_DQS[8:0] SB_DQS#[8:0]	**Data Strobes:** SB_DQS[8:0] and its complement signal group make up a differential strobe pair. The data is captured at the crossing point of SB_DQS[8:0] and its SB_DQS#[8:0] during read and write transactions.	I/O DDR3
SB_DQ[63:0]	**Data Bus:** Channel B data signal interface to the SDRAM data bus.	I/O DDR3
SB_MA[15:0]	**Memory Address:** These signals are used to provide the multiplexed row and column address to the SDRAM.	O DDR3
SB_CK[3:0]	**SDRAM Differential Clock:** Channel B SDRAM Differential clock signal pair. The crossing of the positive edge of SB_CK and the negative edge of its complement SB_CK# are used to sample the command and control signals on the SDRAM.	O DDR3
SB_CK#[3:0]	**SDRAM Inverted Differential Clock:** Channel B SDRAM Differential clock signal-pair complement.	O DDR3
SB_CKE[3:0]	**Clock Enable:** (1 per rank). Used to: • Initialize the SDRAMs during power-up. • Power-down SDRAM ranks. • Place all SDRAM ranks into and out of self-refresh during STR.	O DDR3
SB_CS#[3:0]	**Chip Select:** (1 per rank). Used to select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank.	O DDR3
SB_ODT[3:0]	**On Die Termination:** Active Termination Control.	O DDR3

6.2 Memory Reference and Compensation Signals

Table 6-4. Memory Reference and Compensation

Signal Name	Description	Direction / Buffer Type
SM_VREF	**DDR3 Reference Voltage:** This provides reference voltage to the DDR3 interface and is defined as $V_{DDQ}/2$.	I A

6.3 Reset and Miscellaneous Signals

Table 6-5. Reset and Miscellaneous Signals

Signal Name	Description	Direction / Buffer Type
CFG[17:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. • **CFG[1:0]:** Reserved configuration lane. A test point may be placed on the board for this lane. • **CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal — 1 = Normal operation — 0 = Lane numbers reversed • **CFG[3]:** Reserved • **CFG[4]:** Reserved configuration lane. A test point may be placed on the board for this lane. • **CFG[6:5]:** PCI Express Bifurcation[Note1] — 00 = 1 x8, 2 x4 PCI Express — 01 = Reserved — 10 = 2 x8 PCI Express — 11 = 1 x16 PCI Express • **CFG[17:7]:** Reserved configuration lanes. A test point may be placed on the board for these lands.	I CMOS
FC_x	FC signals are signals that are available for compatibility with other processors. A test point may be placed on the board for these lands.	
PM_SYNC	**Power Management Sync:** A sideband signal to communicate power management status from the platform to the processor.	I CMOS
RESET#	Platform Reset pin driven by the PCH	I CMOS
RSVD RSVD_NCTF	**RESERVED:** All signals that are RSVD and RSVD_NCTF must be left unconnected on the board.	No Connect Non-Critical to Function
SM_DRAMRST#	**DDR3 DRAM Reset:** Reset signal from processor to DRAM devices. One common to all channels.	O CMOS

Notes:
1. PCIe bifurcation support varies with the processor and PCH SKUs used.

6.4 PCI Express*-Based Interface Signals

Table 6-6. PCI Express* Graphics Interface Signals

Signal Name	Description	Direction / Buffer Type
PEG_ICOMPI	**PCI Express Input Current Compensation**	I A
PEG_ICOMPO	**PCI Express Current Compensation**	I A
PEG_RCOMPO	**PCI Express Resistance Compensation**	I A
PEG_RX[15:0] PEG_RX#[15:0] PE_RX[3:0][1] PE_RX#[3:0][1]	**PCI Express Receive Differential Pair**	I PCI Express
PEG_TX[15:0] PEG_TX#[15:0] PE_TX[3:0][1] PE_TX#[3:0][1]	**PCI Express Transmit Differential Pair**	O PCI Express

Notes:

1. PE_TX[3:0] and PE_RX[3:0] are only used for platforms that support 20 PCIe lanes.

6.5 Intel® Flexible Display Interface (Intel® FDI) Signals

Table 6-7. Intel® Flexible Display Interface (Intel® FDI)

Signal Name	Description	Direction / Buffer Type
FDI0_FSYNC[0]	**Intel® Flexible Display Interface Frame Sync** – Pipe A	I CMOS
FDI0_LSYNC[0]	**Intel® Flexible Display Interface Line Sync** – Pipe A	I CMOS
FDI_TX[7:0] FDI_TX#[7:0]	**Intel® Flexible Display Interface Transmit Differential Pairs**	O FDI
FDI1_FSYNC[1]	**Intel® Flexible Display Interface Frame Sync** – Pipe B	I CMOS
FDI1_LSYNC[1]	**Intel® Flexible Display Interface Line Sync** – Pipe B	I CMOS
FDI_INT	**Intel® Flexible Display Interface Hot Plug Interrupt**	I Asynchronous CMOS

6.6 Direct Media Interface (DMI) Signals

Table 6-8. Direct Media Interface (DMI) Signals – Processor to PCH Serial Interface

Signal Name	Description	Direction / Buffer Type
DMI_RX[3:0] DMI_RX#[3:0]	**DMI Input from PCH:** Direct Media Interface receive differential pair.	I DMI
DMI_TX[3:0] DMI_TX#[3:0]	**DMI Output to PCH:** Direct Media Interface transmit differential pair.	O DMI

6.7 Phase Lock Loop (PLL) Signals

Table 6-9. Phase Lock Loop (PLL) Signals

Signal Name	Description	Direction / Buffer Type
BCLK BCLK#	Differential bus clock input to the processor	I Diff Clk

6.8 Test Access Points (TAP) Signals

Table 6-10. Test Access Points (TAP) Signals

Signal Name	Description	Direction / Buffer Type
BPM#[7:0]	**Breakpoint and Performance Monitor Signals:** These signals are outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance.	I/O CMOS
BCLK_ITP BCLK_ITP#	These pins are connected in parallel to the top side debug probe to enable debug capacities.	I
DBR#	DBR# is used only in systems where no debug port is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset.	O
PRDY#	PRDY# is a processor output used by debug tools to determine processor debug readiness.	O Asynchronous CMOS
PREQ#	PREQ# is used by debug tools to request debug operation of the processor.	I Asynchronous CMOS
TCK	**TCK (Test Clock):** This signal provides the clock input for the processor Test Bus (also known as the Test Access Port). TCK must be driven low or allowed to float during power on Reset.	I CMOS
TDI	**TDI (Test Data In):** This signal transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.	I CMOS
TDO	**TDO (Test Data Out):** This signal transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.	O Open Drain
TMS	**TMS (Test Mode Select):** A JTAG specification support signal used by debug tools.	I CMOS
TRST#	**TRST# (Test Reset):** This signal resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset.	I CMOS

6.9 Error and Thermal Protection Signals

Table 6-11. Error and Thermal Protection Signals

Signal Name	Description	Direction / Buffer Type
CATERR#	**Catastrophic Error:** This signal indicates that the system has experienced a catastrophic error and cannot continue to operate. The processor will set this for non-recoverable machine check errors or other unrecoverable internal errors. On the processor, CATERR# is used for signaling the following types of errors: • Legacy MCERRs – CATERR# is asserted for 16 BCLKs. • Legacy IERRs – CATERR# remains asserted until warm or cold reset.	O CMOS
PECI	**PECI (Platform Environment Control Interface):** A serial sideband interface to the processor, it is used primarily for thermal, power, and error management.	I/O Asynchronous
PROCHOT#	**Processor Hot:** PROCHOT# goes active when the processor temperature monitoring sensor(s) detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. This signal can also be driven to the processor to activate the TCC.	CMOS Input/ Open-Drain Output
THERMTRIP#	**Thermal Trip:** The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 130 °C. This is signaled to the system by the THERMTRIP# pin.	O Asynchronous CMOS

6.10 Power Sequencing Signals

Table 6-12. Power Sequencing Signals

Signal Name	Description	Direction / Buffer Type
SM_DRAMPWROK	**SM_DRAMPWROK Processor Input:** Connects to PCH DRAMPWROK.	I Asynchronous CMOS
UNCOREPWRGOOD	The processor requires this input signal to be a clean indication that the V_{CCSA}, V_{CCIO}, V_{AXG}, and V_{DDQ}, power supplies are stable and within specifications. This requirement applies, regardless of the S-state of the processor. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. This is connected to the PCH PROCPWRGD signal.	I Asynchronous CMOS
SKTOCC#	**SKTOCC# (Socket Occupied):** Pulled down directly (0 Ohms) on the processor package to ground. There is no connection to the processor silicon for this signal. System board designers may use this signal to determine if the processor is present.	

6.11 Processor Power Signals

Table 6-13. Processor Power Signals

Signal Name	Description	Direction / Buffer Type
VCC	Processor core power rail	Ref
VCCIO	Processor power for I/O	Ref
VDDQ	Processor I/O supply voltage for DDR3	Ref
VCCAXG	Graphics core power supply.	Ref
VCCPLL	VCCPLL provides isolated power for internal processor PLLs	Ref
VCCSA	System Agent power supply	Ref
VIDSOUT VIDSCLK VIDALERT#	VIDALERT#, VIDSCLK, and VIDSCLK comprise a three signal serial synchronous interface used to transfer power management information between the processor and the voltage regulator controllers. This serial VID interface replaces the parallel VID interface on previous processors.	I/O O I CMOS
VCCSA_VID	**Voltage selection for VCCSA**	O

6.12 Sense Signals

Table 6-14. Sense Signals

Signal Name	Description	Direction / Buffer Type
VCC_SENSE VSS_SENSE	VCC_SENSE and VSS_SENSE provide an isolated, low impedance connection to the processor core voltage and ground. They can be used to sense or measure voltage near the silicon.	O Analog
VAXG_SENSE VSSAXG_SENSE	VAXG_SENSE and VSSAXG_SENSE provide an isolated, low impedance connection to the V_{AXG} voltage and ground. They can be used to sense or measure voltage near the silicon.	O Analog
VCCIO_SENSE VSS_SENSE_VCCIO	VCCIO_SENSE and VSS_SENSE_VCCIO provide an isolated, low impedance connection to the processor V_{CCIO} voltage and ground. They can be used to sense or measure voltage near the silicon.	O Analog
VDDQ_SENSE VSSD_SENSE	VDDQ_SENSE and VSSD_SENSE provides an isolated, low impedance connection to the V_{DDQ} voltage and ground. They can be used to sense or measure voltage near the silicon.	O Analog
VCCSA_SENSE	VCCSA_SENSE provide an isolated, low impedance connection to the processor system agent voltage. It can be used to sense or measure voltage near the silicon.	O Analog

6.13 Ground and Non-Critical to Function (NCTF) Signals

Table 6-15. Ground and Non-Critical to Function (NCTF) Signals

Signal Name	Description	Direction / Buffer Type
VSS	Processor ground node	GND
VSS_NCTF	**Non-Critical to Function:** These pins are for package mechanical reliability.	

6.14 Processor Internal Pull-Up / Pull-Down Resistors

Table 6-16. Processor Internal Pull-Up / Pull-Down Resistors

Signal Name	Pull-Up / Pull-Down	Rail	Value
BPM[7:0]	Pull Up	VCCIO	65–165 Ω
PRDY#	Pull Up	VCCIO	65–165 Ω
PREQ#	Pull Up	VCCIO	65–165 Ω
TCK	Pull Down	VSS	5–15 kΩ
TDI	Pull Up	VCCIO	5–15 kΩ
TMS	Pull Up	VCCIO	5–15 kΩ
TRST#	Pull Up	VCCIO	5–15 kΩ
CFG[17:0]	Pull Up	VCCIO	5–15 kΩ

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7 Electrical Specifications

7.1 Power and Ground Lands

The processor has VCC, VDDQ, VCCPLL, VCCSA, VCCAXG, VCCIO and VSS (ground) inputs for on-chip power distribution. All power lands must be connected to their respective processor power planes, while all VSS lands must be connected to the system ground plane. Use of multiple power and ground planes is recommended to reduce I*R drop. The VCC and VCCAXG lands must be supplied with the voltage determined by the processor **S**erial **V**oltage **ID**entification (SVID) interface. A new serial VID interface is implemented on the processor. Table 7-1 specifies the voltage level for the various VIDs.

7.2 Decoupling Guidelines

Due to its large number of transistors and high internal clock speeds, the processor is capable of generating large current swings between low- and full-power states. This may cause voltages on power planes to sag below their minimum values, if bulk decoupling is not adequate. Larger bulk storage (C_{BULK}), such as electrolytic capacitors, supply current during longer lasting changes in current demand (for example, coming out of an idle condition). Similarly, capacitors act as a storage well for current when entering an idle condition from a running condition. To keep voltages within specification, output decoupling must be properly designed.

Caution: Design the board to ensure that the voltage provided to the processor remains within the specifications listed in Table 7-5. Failure to do so can result in timing violations or reduced lifetime of the processor.

7.2.1 Voltage Rail Decoupling

The voltage regulator solution needs to provide:

- bulk capacitance with low effective series resistance (ESR).
- a low interconnect resistance from the regulator to the socket.
- bulk decoupling to compensate for large current swings generated during poweron, or low-power idle state entry/exit.

The power delivery solution must ensure that the voltage and current specifications are met, as defined in Table 7-5.

7.3 Processor Clocking (BCLK[0], BCLK#[0])

The processor uses a differential clock to generate the processor core operating frequency, memory controller frequency, system agent frequencies, and other internal clocks. The processor core frequency is determined by multiplying the processor core ratio by the BCLK frequency. Clock multiplying within the processor is provided by an internal phase locked loop (PLL) that requires a constant frequency input, with exceptions for Spread Spectrum Clocking (SSC).

The processor's maximum non-turbo core frequency is configured during power-on reset by using its manufacturing default value. This value is the highest non-turbo core multiplier at which the processor can operate. If lower maximum speeds are desired, the appropriate ratio can be configured using the FLEX_RATIO MSR.

7.3.1 Phase Lock Loop (PLL) Power Supply

An on-die PLL filter solution is implemented on the processor. Refer to Table 7-6 for DC specifications.

7.4 V_{CC} Voltage Identification (VID)

The processor uses three signals for the serial voltage identification interface to support automatic selection of voltages. Table 7-1 specifies the voltage level corresponding to the eight bit VID value transmitted over serial VID. A '1' in this table refers to a high voltage level and a '0' refers to a low voltage level. If the voltage regulation circuit cannot supply the voltage that is requested, the voltage regulator must disable itself. VID signals are CMOS push/pull drivers. Refer to Table 7-9 for the DC specifications for these signals. The VID codes will change due to temperature and/or current load changes in order to minimize the power of the part. A voltage range is provided in Table 7-5. The specifications are set so that one voltage regulator can operate with all supported frequencies.

Individual processor VID values may be set during manufacturing so that two devices at the same core frequency may have different default VID settings. This is shown in the VID range values in Table 7-5. The processor provides the ability to operate while transitioning to an adjacent VID and its associated voltage. This will represent a DC shift in the loadline.

See the *VR12/IMVP7 SVID Protocol* for further details.

Table 7-1. VR 12.0 Voltage Identification Definition (Sheet 1 of 3)

VID 7	VID 6	VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	HEX		V_{CC_MAX}
0	0	0	0	0	0	0	0	0	0	0.00000
0	0	0	0	0	0	0	1	0	1	0.25000
0	0	0	0	0	0	1	0	0	2	0.25500
0	0	0	0	0	0	1	1	0	3	0.26000
0	0	0	0	0	1	0	0	0	4	0.26500
0	0	0	0	0	1	0	1	0	5	0.27000
0	0	0	0	0	1	1	0	0	6	0.27500
0	0	0	0	0	1	1	1	0	7	0.28000
0	0	0	0	1	0	0	0	0	8	0.28500
0	0	0	0	1	0	0	1	0	9	0.29000
0	0	0	0	1	0	1	0	0	A	0.29500
0	0	0	0	1	0	1	1	0	B	0.30000
0	0	0	0	1	1	0	0	0	C	0.30500
0	0	0	0	1	1	0	1	0	D	0.31000
0	0	0	0	1	1	1	0	0	E	0.31500
0	0	0	0	1	1	1	1	0	F	0.32000
0	0	0	1	0	0	0	0	1	0	0.32500
0	0	0	1	0	0	0	1	1	1	0.33000
0	0	0	1	0	0	1	0	1	2	0.33500
0	0	0	1	0	0	1	1	1	3	0.34000
0	0	0	1	0	1	0	0	1	4	0.34500
0	0	0	1	0	1	0	1	1	5	0.35000
0	0	0	1	0	1	1	0	1	6	0.35500
0	0	0	1	0	1	1	1	1	7	0.36000
0	0	0	1	1	0	0	0	1	8	0.36500
0	0	0	1	1	0	0	1	1	9	0.37000
0	0	0	1	1	0	1	0	1	A	0.37500
0	0	0	1	1	0	1	1	1	B	0.38000
0	0	0	1	1	1	0	0	1	C	0.38500
0	0	0	1	1	1	0	1	1	D	0.39000
0	0	0	1	1	1	1	0	1	E	0.39500
0	0	0	1	1	1	1	1	1	F	0.40000
0	0	1	0	0	0	0	0	2	0	0.40500
0	0	1	0	0	0	0	1	2	1	0.41000
0	0	1	0	0	0	1	0	2	2	0.41500
0	0	1	0	0	0	1	1	2	3	0.42000
0	0	1	0	0	1	0	0	2	4	0.42500
0	0	1	0	0	1	0	1	2	5	0.43000
0	0	1	0	0	1	1	0	2	6	0.43500
0	0	1	0	0	1	1	1	2	7	0.44000
0	0	1	0	1	0	0	0	2	8	0.44500
0	0	1	0	1	0	0	1	2	9	0.45000
0	0	1	0	1	0	1	0	2	A	0.45500
1	0	0	0	0	0	0	0	8	0	0.88500
1	0	0	0	0	0	0	1	8	1	0.89000
1	0	0	0	0	0	1	0	8	2	0.89500
1	0	0	0	0	0	1	1	8	3	0.90000
1	0	0	0	0	1	0	0	8	4	0.90500
1	0	0	0	0	1	0	1	8	5	0.91000
1	0	0	0	0	1	1	0	8	6	0.91500
1	0	0	0	0	1	1	1	8	7	0.92000
1	0	0	0	1	0	0	0	8	8	0.92500
1	0	0	0	1	0	0	1	8	9	0.93000
1	0	0	0	1	0	1	0	8	A	0.93500
1	0	0	0	1	0	1	1	8	B	0.94000
1	0	0	0	1	1	0	0	8	C	0.94500
1	0	0	0	1	1	0	1	8	D	0.95000
1	0	0	0	1	1	1	0	8	E	0.95500
1	0	0	0	1	1	1	1	8	F	0.96000
1	0	0	1	0	0	0	0	9	0	0.96500
1	0	0	1	0	0	0	1	9	1	0.97000
1	0	0	1	0	0	1	0	9	2	0.97500
1	0	0	1	0	0	1	1	9	3	0.98000
1	0	0	1	0	1	0	0	9	4	0.98500
1	0	0	1	0	1	0	1	9	5	0.99000
1	0	0	1	0	1	1	0	9	6	0.99500
1	0	0	1	0	1	1	1	9	7	1.00000
1	0	0	1	1	0	0	0	9	8	1.00500
1	0	0	1	1	0	0	1	9	9	1.01000
1	0	0	1	1	0	1	0	9	A	1.01500
1	0	0	1	1	0	1	1	9	B	1.02000
1	0	0	1	1	1	0	0	9	C	1.02500
1	0	0	1	1	1	0	1	9	D	1.03000
1	0	0	1	1	1	1	0	9	E	1.03500
1	0	0	1	1	1	1	1	9	F	1.04000
1	0	1	0	0	0	0	0	A	0	1.04500
1	0	1	0	0	0	0	1	A	1	1.05000
1	0	1	0	0	0	1	0	A	2	1.05500
1	0	1	0	0	0	1	1	A	3	1.06000
1	0	1	0	0	1	0	0	A	4	1.06500
1	0	1	0	0	1	0	1	A	5	1.07000
1	0	1	0	0	1	1	0	A	6	1.07500
1	0	1	0	0	1	1	1	A	7	1.08000
1	0	1	0	1	0	0	0	A	8	1.08500
1	0	1	0	1	0	0	1	A	9	1.09000
1	0	1	0	1	0	1	0	A	A	1.09500

Table 7-1. VR 12.0 Voltage Identification Definition (Sheet 2 of 3)

VID 7	VID 6	VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	HEX		V_{CC_MAX}
0	0	1	0	1	0	1	1	2	B	0.46000
0	0	1	0	1	1	0	0	2	C	0.46500
0	0	1	0	1	1	0	1	2	D	0.47000
0	0	1	0	1	1	1	0	2	E	0.47500
0	0	1	0	1	1	1	1	2	F	0.48000
0	0	1	1	0	0	0	0	3	0	0.48500
0	0	1	1	0	0	0	1	3	1	0.49000
0	0	1	1	0	0	1	0	3	2	0.49500
0	0	1	1	0	0	1	1	3	3	0.50000
0	0	1	1	0	1	0	0	3	4	0.50500
0	0	1	1	0	1	0	1	3	5	0.51000
0	0	1	1	0	1	1	0	3	6	0.51500
0	0	1	1	0	1	1	1	3	7	0.52000
0	0	1	1	1	0	0	0	3	8	0.52500
0	0	1	1	1	0	0	1	3	9	0.53000
0	0	1	1	1	0	1	0	3	A	0.53500
0	0	1	1	1	0	1	1	3	B	0.54000
0	0	1	1	1	1	0	0	3	C	0.54500
0	0	1	1	1	1	0	1	3	D	0.55000
0	0	1	1	1	1	1	0	3	E	0.55500
0	0	1	1	1	1	1	1	3	F	0.56000
0	1	0	0	0	0	0	0	4	0	0.56500
0	1	0	0	0	0	0	1	4	1	0.57000
0	1	0	0	0	0	1	0	4	2	0.57500
0	1	0	0	0	0	1	1	4	3	0.58000
0	1	0	0	0	1	0	0	4	4	0.58500
0	1	0	0	0	1	0	1	4	5	0.59000
0	1	0	0	0	1	1	0	4	6	0.59500
0	1	0	0	0	1	1	1	4	7	0.60000
0	1	0	0	1	0	0	0	4	8	0.60500
0	1	0	0	1	0	0	1	4	9	0.61000
0	1	0	0	1	0	1	0	4	A	0.61500
0	1	0	0	1	0	1	1	4	B	0.62000
0	1	0	0	1	1	0	0	4	C	0.62500
0	1	0	0	1	1	0	1	4	D	0.63000
0	1	0	0	1	1	1	0	4	E	0.63500
0	1	0	0	1	1	1	1	4	F	0.64000
0	1	0	1	0	0	0	0	5	0	0.64500
0	1	0	1	0	0	0	1	5	1	0.65000
0	1	0	1	0	0	1	0	5	2	0.65500
0	1	0	1	0	0	1	1	5	3	0.66000
0	1	0	1	0	1	0	0	5	4	0.66500
0	1	0	1	0	1	0	1	5	5	0.67000
1	0	1	0	1	0	1	1	A	B	1.10000
1	0	1	0	1	1	0	0	A	C	1.10500
1	0	1	0	1	1	0	1	A	D	1.11000
1	0	1	0	1	1	1	0	A	E	1.11500
1	0	1	0	1	1	1	1	A	F	1.12000
1	0	1	1	0	0	0	0	B	0	1.12500
1	0	1	1	0	0	0	1	B	1	1.13000
1	0	1	1	0	0	1	0	B	2	1.13500
1	0	1	1	0	0	1	1	B	3	1.14000
1	0	1	1	0	1	0	0	B	4	1.14500
1	0	1	1	0	1	0	1	B	5	1.15000
1	0	1	1	0	1	1	0	B	6	1.15500
1	0	1	1	0	1	1	1	B	7	1.16000
1	0	1	1	1	0	0	0	B	8	1.16500
1	0	1	1	1	0	0	1	B	9	1.17000
1	0	1	1	1	0	1	0	B	A	1.17500
1	0	1	1	1	0	1	1	B	B	1.18000
1	0	1	1	1	1	0	0	B	C	1.18500
1	0	1	1	1	1	0	1	B	D	1.19000
1	0	1	1	1	1	1	0	B	E	1.19500
1	0	1	1	1	1	1	1	B	F	1.20000
1	1	0	0	0	0	0	0	C	0	1.20500
1	1	0	0	0	0	0	1	C	1	1.21000
1	1	0	0	0	0	1	0	C	2	1.21500
1	1	0	0	0	0	1	1	C	3	1.22000
1	1	0	0	0	1	0	0	C	4	1.22500
1	1	0	0	0	1	0	1	C	5	1.23000
1	1	0	0	0	1	1	0	C	6	1.23500
1	1	0	0	0	1	1	1	C	7	1.24000
1	1	0	0	1	0	0	0	C	8	1.24500
1	1	0	0	1	0	0	1	C	9	1.25000
1	1	0	0	1	0	1	0	C	A	1.25500
1	1	0	0	1	0	1	1	C	B	1.26000
1	1	0	0	1	1	0	0	C	C	1.26500
1	1	0	0	1	1	0	1	C	D	1.27000
1	1	0	0	1	1	1	0	C	E	1.27500
1	1	0	0	1	1	1	1	C	F	1.28000
1	1	0	1	0	0	0	0	D	0	1.28500
1	1	0	1	0	0	0	1	D	1	1.29000
1	1	0	1	0	0	1	0	D	2	1.29500
1	1	0	1	0	0	1	1	D	3	1.30000
1	1	0	1	0	1	0	0	D	4	1.30500
1	1	0	1	0	1	0	1	D	5	1.31000

Table 7-1. VR 12.0 Voltage Identification Definition (Sheet 3 of 3)

VID 7	VID 6	VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	HEX		V_{CC_MAX}
0	1	0	1	0	1	1	0	5	6	0.67500
0	1	0	1	0	1	1	1	5	7	0.68000
0	1	0	1	1	0	0	0	5	8	0.68500
0	1	0	1	1	0	0	1	5	9	0.69000
0	1	0	1	1	0	1	0	5	A	0.69500
0	1	0	1	1	0	1	1	5	B	0.70000
0	1	0	1	1	1	0	0	5	C	0.70500
0	1	0	1	1	1	0	1	5	D	0.71000
0	1	0	1	1	1	1	0	5	E	0.71500
0	1	0	1	1	1	1	1	5	F	0.72000
0	1	1	0	0	0	0	0	6	0	0.72500
0	1	1	0	0	0	0	1	6	1	0.73000
0	1	1	0	0	0	1	0	6	2	0.73500
0	1	1	0	0	0	1	1	6	3	0.74000
0	1	1	0	0	1	0	0	6	4	0.74500
0	1	1	0	0	1	0	1	6	5	0.75000
0	1	1	0	0	1	1	0	6	6	0.75500
0	1	1	0	0	1	1	1	6	7	0.76000
0	1	1	0	1	0	0	0	6	8	0.76500
0	1	1	0	1	0	0	1	6	9	0.77000
0	1	1	0	1	0	1	0	6	A	0.77500
0	1	1	0	1	0	1	1	6	B	0.78000
0	1	1	0	1	1	0	0	6	C	0.78500
0	1	1	0	1	1	0	1	6	D	0.79000
0	1	1	0	1	1	1	0	6	E	0.79500
0	1	1	0	1	1	1	1	6	F	0.80000
0	1	1	1	0	0	0	0	7	0	0.80500
0	1	1	1	0	0	0	1	7	1	0.81000
0	1	1	1	0	0	1	0	7	2	0.81500
0	1	1	1	0	0	1	1	7	3	0.82000
0	1	1	1	0	1	0	0	7	4	0.82500
0	1	1	1	0	1	0	1	7	5	0.83000
0	1	1	1	0	1	1	0	7	6	0.83500
0	1	1	1	0	1	1	1	7	7	0.84000
0	1	1	1	1	0	0	0	7	8	0.84500
0	1	1	1	1	0	0	1	7	9	0.85000
0	1	1	1	1	0	1	0	7	A	0.85500
0	1	1	1	1	0	1	1	7	B	0.86000
0	1	1	1	1	1	0	0	7	C	0.86500
0	1	1	1	1	1	0	1	7	D	0.87000
0	1	1	1	1	1	1	0	7	E	0.87500
0	1	1	1	1	1	1	1	7	F	0.88000
1	1	0	1	0	1	1	0	D	6	1.31500
1	1	0	1	0	1	1	1	D	7	1.32000
1	1	0	1	1	0	0	0	D	8	1.32500
1	1	0	1	1	0	0	1	D	9	1.33000
1	1	0	1	1	0	1	0	D	A	1.33500
1	1	0	1	1	0	1	1	D	B	1.34000
1	1	0	1	1	1	0	0	D	C	1.34500
1	1	0	1	1	1	0	1	D	D	1.35000
1	1	0	1	1	1	1	0	D	E	1.35500
1	1	0	1	1	1	1	1	D	F	1.36000
1	1	1	0	0	0	0	0	E	0	1.36500
1	1	1	0	0	0	0	1	E	1	1.37000
1	1	1	0	0	0	1	0	E	2	1.37500
1	1	1	0	0	0	1	1	E	3	1.38000
1	1	1	0	0	1	0	0	E	4	1.38500
1	1	1	0	0	1	0	1	E	5	1.39000
1	1	1	0	0	1	1	0	E	6	1.39500
1	1	1	0	0	1	1	1	E	7	1.40000
1	1	1	0	1	0	0	0	E	8	1.40500
1	1	1	0	1	0	0	1	E	9	1.41000
1	1	1	0	1	0	1	0	E	A	1.41500
1	1	1	0	1	0	1	1	E	B	1.42000
1	1	1	0	1	1	0	0	E	C	1.42500
1	1	1	0	1	1	0	1	E	D	1.43000
1	1	1	0	1	1	1	0	E	E	1.43500
1	1	1	0	1	1	1	1	E	F	1.44000
1	1	1	1	0	0	0	0	F	0	1.44500
1	1	1	1	0	0	0	1	F	1	1.45000
1	1	1	1	0	0	1	0	F	2	1.45500
1	1	1	1	0	0	1	1	F	3	1.46000
1	1	1	1	0	1	0	0	F	4	1.46500
1	1	1	1	0	1	0	1	F	5	1.47000
1	1	1	1	0	1	1	0	F	6	1.47500
1	1	1	1	0	1	1	1	F	7	1.48000
1	1	1	1	1	0	0	0	F	8	1.48500
1	1	1	1	1	0	0	1	F	9	1.49000
1	1	1	1	1	0	1	0	F	A	1.49500
1	1	1	1	1	0	1	1	F	B	1.50000
1	1	1	1	1	1	0	0	F	C	1.50500
1	1	1	1	1	1	0	1	F	D	1.51000
1	1	1	1	1	1	1	0	F	E	1.51500
1	1	1	1	1	1	1	1	F	F	1.52000

7.5 System Agent (SA) VCC VID

The VCC_{SA} is configured by the processor output pin VCCSA_VID.

VCCSA_VID output default logic state is low for the processors; logic high is reserved for future compatibility.

Table 7-2 specifies the different VCCSA_VID configurations.

Table 7-2. VCCSA_VID configuration

Processor Family	VCCSA_VID	Selected VCCSA
2nd Generation Intel® Core™ processor family desktop, Intel® Pentium® processor family desktop, Intel® Celeron® processor family desktop	0	0.925 V
Future Intel processors	1	Note 1

Notes:

1. Some of V_{CCSA} configurations are reserved for future Intel processor families.

7.6 Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD – These signals should not be connected.
- RSVD_NCTF – These signals are non-critical to function and may be left un-connected

Arbitrary connection of these signals to V_{CC}, V_{CCIO}, V_{DDQ}, V_{CCPLL}, V_{CCSA}, V_{CCAXG}, V_{SS}, or to any other signal (including each other) may result in component malfunction or incompatibility with future processors. See Chapter 8 for a land listing of the processor and the location of all reserved signals.

For reliable operation, always connect unused inputs or bi-directional signals to an appropriate signal level. Unused active high inputs should be connected through a resistor to ground (V_{SS}). Unused outputs maybe left unconnected; however, this may interfere with some Test Access Port (TAP) functions, complicate debug probing, and prevent boundary scan testing. A resistor must be used when tying bi-directional signals to power or ground. When tying any signal to power or ground, a resistor will also allow for system testability. For details see Table 7-9.

7.7 Signal Groups

Signals are grouped by buffer type and similar characteristics as listed in Table 7-3. The buffer type indicates which signaling technology and specifications apply to the signals. All the differential signals, and selected DDR3 and Control Sideband signals have On-Die Termination (ODT) resistors. There are some signals that do not have ODT and need to be terminated on the board.

Table 7-3. Signal Groups (Sheet 1 of 2)[1]

Signal Group	Type	Signals
System Reference Clock		
Differential	CMOS Input	BCLK[0], BCLK#[0]
DDR3 Reference Clocks[2]		
Differential	DDR3 Output	SA_CK[3:0], SA_CK#[3:0] SB_CK[3:0], SB_CK#[3:0]
DDR3 Command Signals[2]		
Single Ended	DDR3 Output	SA_RAS#, SB_RAS#, SA_CAS#, SB_CAS# SA_WE#, SB_WE# SA_MA[15:0], SB_MA[15:0] SA_BS[2:0], SB_BS[2:0] SM_DRAMRST# SA_CS#[3:0], SB_CS#[3:0] SA_ODT[3:0], SB_ODT[3:0] SA_CKE[3:0], SB_CKE[3:0]
DDR3 Data Signals[2]		
Single ended	DDR3 Bi-directional	SA_DQ[63:0], SB_DQ[63:0]
Differential	DDR3 Bi-directional	SA_DQS[8:0], SA_DQS#[8:0] SB_DQS[8:0], SB_DQS#[8:0]
TAP (ITP/XDP)		
Single Ended	CMOS Input	TCK, TDI, TMS, TRST#
Single Ended	CMOS Output	TDO
Single Ended	Asynchronous CMOS Output	TAPPWRGOOD
Control Sideband		
Single Ended	CMOS Input	CFG[17:0]
Single Ended	Asynchronous CMOS/Open Drain Bi-directional	PROCHOT#
Single Ended	Asynchronous CMOS Output	THERMTRIP#, CATERR#
Single Ended	Asynchronous CMOS Input	SM_DRAMPWROK, UNCOREPWRGOOD[3], PM_SYNC, RESET#
Single Ended	Asynchronous Bi-directional	PECI
Single Ended	CMOS Input Open Drain Output Bi-directional CMOS Input /Open Drain Output	VIDALERT# VIDSCLK VIDSOUT
Power/Ground/Other		
	Power	VCC, VCC_NCTF, VCCIO, VCCPLL, VDDQ, VCCAXG
	Ground	VSS
	No Connect and test point	RSVD, RSVD_NCTF, RSVD_TP, FC_x

Table 7-3. Signal Groups (Sheet 2 of 2)[1]

Signal Group	Type	Signals
	Sense Points	VCC_SENSE, VSS_SENSE, VCCIO_SENSE, VSS_SENSE_VCCIO, VAXG_SENSE, VSSAXG_SENSE
	Other	SKTOCC#, DBR#
PCI Express*		
Differential	PCI Express Input	PEG_RX[15:0], PEG_RX#[15:0], PE_RX[3:0], PE_RX#[3:0]
Differential	PCI Express Output	PEG_TX[15:0], PEG_TX#[15:0], PE_TX[3:0], PE_TX#[3:0]
Single Ended	Analog Input	PEG_ICOMP0, PEG_COMPI, PEG_RCOMP0
DMI		
Differential	DMI Input	DMI_RX[3:0], DMI_RX#[3:0]
Differential	DMI Output	DMI_TX[3:0], DMI_TX#[3:0]
Intel® FDI		
Single Ended	FDI Input	FDI_FSYNC[1:0], FDI_LSYNC[1:0], FDI_INT
Differential	FDI Output	FDI_TX[7:0], FDI_TX#[7:0]
Single Ended	Analog Input	FDI_COMPIO, FDI_ICOMPO

Notes:
1. Refer to Chapter 6 and Chapter 8 for signal description details.
2. SA and SB refer to DDR3 Channel A and DDR3 Channel B.
3. The maximum rise/fall time for UNCOREPWRGOOD is 20 ns.

All Control Sideband Asynchronous signals are required to be asserted/de-asserted for at least **10 BCLKs** with a maximum Trise/Tfall of 6 ns for the processor to recognize the proper signal state. See Section 7.10 for the DC specifications.

7.8 Test Access Port (TAP) Connection

Due to the voltage levels supported by other components in the Test Access Port (TAP) logic, Intel recommends the processor be first in the TAP chain, followed by any other components within the system. A translation buffer should be used to connect to the rest of the chain unless one of the other components is capable of accepting an input of the appropriate voltage. Two copies of each signal may be required with each driving a different voltage level.

The processor supports Boundary Scan (JTAG) IEEE 1149.1-2001 and IEEE 1149.6-2003 standards. Some small portion of the I/O pins may support only one of these standards.

7.9 Storage Conditions Specifications

Environmental storage condition limits define the temperature and relative humidity that the device is exposed to while being stored in a moisture barrier bag. The specified storage conditions are for component level prior to board attach.

Table 7-4 specifies absolute maximum and minimum storage temperature limits that represent the maximum or minimum device condition beyond which damage, latent or otherwise, may occur. The table also specifies sustained storage temperature, relative humidity, and time-duration limits. These limits specify the maximum or minimum device storage conditions for a sustained period of time. Failure to adhere to the following specifications can affect long term reliability of the processor.

Table 7-4. Storage Condition Ratings

Symbol	Parameter	Min	Max	Notes
$T_{\text{absolute storage}}$	The non-operating device storage temperature. Damage (latent or otherwise) may occur when exceeded for any length of time.	-25 °C	125 °C	1, 2, 3, 4
$T_{\text{sustained storage}}$	The ambient storage temperature (in shipping media) for a sustained period of time	-5 °C	40 °C	5, 6
$T_{\text{short term storage}}$	The ambient storage temperature (in shipping media) for a short period of time.	-20 °C	85 °C	
$RH_{\text{sustained storage}}$	The maximum device storage relative humidity for a sustained period of time.	60% at 24 °C		6, 7
$Time_{\text{sustained storage}}$	A prolonged or extended period of time; typically associated with customer shelf life.	0 Months	30 Months	7
$Time_{\text{short term storage}}$	A short-period of time.	0 hours	72 hours	

Notes:

1. Refers to a component device that is not assembled in a board or socket and is not electrically connected to a voltage reference or I/O signal.
2. Specified temperatures are not to exceed values based on data collected. Exceptions for surface mount reflow are specified by the applicable JEDEC standard. Non-adherence may affect processor reliability.
3. $T_{\text{absolute storage}}$ applies to the unassembled component only and does not apply to the shipping media, moisture barrier bags, or desiccant.
4. Component product device storage temperature qualification methods may follow JESD22-A119 (low temp) and JESD22-A103 (high temp) standards when applicable for volatile memory.
5. Intel branded products are specified and certified to meet the following temperature and humidity limits that are given as an example only (Non-Operating Temperature Limit: -40 °C to 70 °C and Humidity: 50% to 90%, non-condensing with a maximum wet bulb of 28 °C.) Post board attach storage temperature limits are not specified for non-Intel branded boards.
6. The JEDEC J-JSTD-020 moisture level rating and associated handling practices apply to all moisture sensitive devices removed from the moisture barrier bag.
7. Nominal temperature and humidity conditions and durations are given and tested within the constraints imposed by $T_{\text{sustained storage}}$ and customer shelf life in applicable Intel boxes and bags.

7.10 DC Specifications

The processor DC specifications in this section are defined at the processor pads, unless noted otherwise. See Chapter 8 for the processor land listings and Chapter 6 for signal definitions. Voltage and current specifications are detailed in Table 7-5, Table 7-6, and Table 7-7.

The DC specifications for the DDR3 signals are listed in Table 7-8 Control Sideband and Test Access Port (TAP) are listed in Table 7-9.

Table 7-5 through Table 7-7 list the DC specifications for the processor and are valid only while meeting the thermal specifications (as specified in the Thermal / Mechanical Specifications and Guidelines), clock frequency, and input voltages. Care should be taken to read all notes associated with each parameter.

7.10.1 Voltage and Current Specifications

Table 7-5. Processor Core Active and Idle Mode DC Voltage and Current Specifications (Sheet 1 of 2)

Symbol	Parameter	Min	Typ	Max	Unit	Note[1]
VID	VID Range	0.2500	—	1.5200	V	2
LL_{VCC}	V_{CC} Loadline Slope 2011D, 2011C, 2011B (processors with 95 W, 65 W, and 45 W TDPs)		1.7		mΩ	3, 5, 6
V_{CC}TOB	V_{CC} Tolerance Band 2011D, 2011C, 2011B (processors with 95 W, 65 W, and 45 W TDPs) PS0 PS1 PS2		±16 ±13 ±11.5		mV	3, 5, 6, 7
V_{CC}Ripple	Ripple: 2011D, 2011C, 2011B (processors with 95 W, 65 W, and 45 W TDPs) PS0 PS1 PS2		±7 ±10 -10/+25		mV	3, 5, 6, 7
LL_{VCC}	V_{CC} Loadline Slope 2011A (processors with 35 W TDP)		2.9		mΩ	3, 5, 6, 8
V_{CC}TOB	V_{CC} Tolerance Band 2011A (processors with 35 W TDP) PS0 PS1 PS2		19 19 11.5		mV	3, 5, 6, 7, 8
V_{CC}Ripple	Ripple: 2011A (processors with 35 W TDP) PS0 PS1 PS2		±10 ±10 -10/+25		mV	3, 5, 6, 7, 8
$V_{CC,BOOT}$	Default V_{CC} voltage for initial power up	—	0	—	V	
I_{CC}	2011D (processors with 95 W TDPs) I_{CC}	—	—	112	A	4
I_{CC}	2011C (processors with 65 W TDP) I_{CC}	—	—	75	A	4

Table 7-5. Processor Core Active and Idle Mode DC Voltage and Current Specifications (Sheet 2 of 2)

Symbol	Parameter	Min	Typ	Max	Unit	Note[1]
I_{CC}	2011B (processors with 45 W TDP) I_{CC}	—	—	60	A	4
I_{CC}	2011A (processors with 35 W TDP) I_{CC}	—	—	35	A	4
I_{CC_TDC}	2011D (processors with 95 W TDPs) Sustained I_{CC}	—	—	85	A	4
I_{CC_TDC}	2011C (processors with 65 W TDP) Sustained I_{CC}	—	—	55	A	4
I_{CC_TDC}	2011B (processors with 45 W TDP) Sustained I_{CC}	—	—	40	A	4
I_{CC_TDC}	2011A (processors with 35 W TDP) Sustained I_{CC}	—	—	25	A	4

Notes:
1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
2. Each processor is programmed with a maximum valid voltage identification value (VID) that is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Note that this differs from the VID employed by the processor during a power management event (Adaptive Thermal Monitor, Enhanced Intel SpeedStep Technology, or Low Power States).
3. The voltage specification requirements are measured across VCC_SENSE and VSS_SENSE lands at the socket with a 20-MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1-MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.
4. ICC_MAX specification is based on the V_{CC} loadline at worst case (highest) tolerance and ripple.
5. The V_{CC} specifications represent static and transient limits.
6. The loadlines specify voltage limits at the die measured at the VCC_SENSE and VSS_SENSE lands. Voltage regulation feedback for voltage regulator circuits must also be taken from processor VCC_SENSE and VSS_SENSE lands.
7. PSx refers to the voltage regulator power state as set by the SVID protocol.
8. 2011A (processors with 35 W TDP) loadline slope, TOB, and ripple specifications allow for a cost reduced voltage regulator for boards supporting only the 2011A (processors with 35 W TDP). 2011A (processors with 35 W TDP) processors may also use the loadline slope, TOB, and ripple specifications for the 2011D (processors with 95 W TDP), 2011C (processors with 65 W TDP), and 2011B (processors with 45 W TDP).

Table 7-6. Processor System Agent I/O Buffer Supply DC Voltage and Current Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Note [1]
V_{CCSA}	Voltage for the system agent	0.879	0.925	0.971	V	2
V_{DDQ}	Processor I/O supply voltage for DDR3	1.425	1.5	1.575	V	
V_{CCPLL}	PLL supply voltage (DC + AC specification)	1.71	1.8	1.89	V	
V_{CCIO}	Processor I/O supply voltage for other than DDR3	-2/-3%	1.05	+2/+3%	V	3
I_{SA}	Current for the system agent	—	—	8.8	A	
I_{SA_TDC}	Sustained current for the system agent	—	—	8.2	A	
I_{DDQ}	Processor I/O supply current for DDR3	—	—	4.75	A	
I_{DDQ_TDC}	Processor I/O supply sustained current for DDR3	—	—	4.75	A	
$I_{DDQ\_STANDBY}$	Processor I/O supply standby current for DDR3	—	—	1	A	
I_{CC_VCCPLL}	PLL supply current	—	—	1.5	A	
$I_{CC\_VCCPLL\_TDC}$	PLL sustained supply current	—	—	0.93	A	
I_{CC_VCCIO}	Processor I/O supply current	—	—	8.5	A	
$I_{CC\_VCCIO\_TDC}$	Processor I/O supply sustained current	—	—	8.5	A	

Notes:

1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
2. V_{CCSA} must be provided using a separate voltage source and not be connected to V_{CC}. This specification is measured at VCCSA_SENSE.
3. ±5% total. Minimum of ±2% DC and 3% AC at the sense point. di/dt = 50 A/us with 150 ns step.

Table 7-7. Processor Graphics VID based (V_{AXG}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Note[2]
V_{AXG} GFX_VID Range	GFX_VID Range for V_{CCAXG}	0.2500	—	1.5200	V	1
LL_{AXG}	V_{CCAXG} Loadline Slope	4.1			mΩ	3, 4
V_{AXG}TOB	V_{CC} Tolerance Band PS0, PS1 PS2	 19 11.5			mV	3, 4, 5
V_{AXG}Ripple	Ripple: PS0 PS1 PS2	 ±10 ±10 -10/+15			mV	3, 4, 5
I_{AXG}	Current for Processor Graphics core	—	—	35	A	
I_{AXG_TDC}	Sustained current for Processor Graphics core	—	—	25	A	

Notes:

1. V_{CCAXG} is VID based rail.
2. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
3. The V_{AXG_MIN} and V_{AXG_MAX} loadlines represent static and transient limits.
4. The loadlines specify voltage limits at the die measured at the VAXG_SENSE and VSSAXG_SENSE lands. Voltage regulation feedback for voltage regulator circuits must also be taken from processor VAXG_SENSE and VSSAXG_SENSE lands.
5. PSx refers to the voltage regulator power state as set by the SVID protocol.
6. Each processor is programmed with a maximum valid voltage identification value (VID) that is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Note that this differs from the VID employed by the processor during a power management event (Adaptive Thermal Monitor, Enhanced Intel SpeedStep Technology, or Low Power States).

Table 7-8. DDR3 Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes[1,9]
V_{IL}	Input Low Voltage	—	—	SM_VREF – 0.1	V	2,4
V_{IH}	Input High Voltage	SM_VREF + 0.1	—	—	V	3
V_{OL}	Output Low Voltage	—	$(V_{DDQ} / 2)^* (R_{ON} /(R_{ON}+R_{TERM}))$	—		6
V_{OH}	Output High Voltage	—	$V_{DDQ} – ((V_{DDQ} / 2)^* (R_{ON}/(R_{ON}+R_{TERM}))$	—	V	4,6
$R_{ON\_UP(DQ)}$	DDR3 data buffer pull-up resistance	24.31	28.6	32.9	Ω	5
$R_{ON\_DN(DQ)}$	DDR3 data buffer pull-down resistance	22.88	28.6	34.32	Ω	5
$R_{ODT(DQ)}$	DDR3 on-die termination equivalent resistance for data signals	83 41.5	100 50	117 65	Ω	7
$V_{ODT(DC)}$	DDR3 on-die termination DC working point (driver set to receive mode)	0.43*V_{DDQ}	0.5*V_{DDQ}	0.56*V_{CC}	V	7
$R_{ON\_UP(CK)}$	DDR3 clock buffer pull-up resistance	20.8	26	28.6	Ω	5
$R_{ON\_DN(CK)}$	DDR3 clock buffer pull-down resistance	20.8	26	31.2	Ω	5
$R_{ON\_UP(CMD)}$	DDR3 command buffer pull-up resistance	16	20	23	Ω	5
$R_{ON\_DN(CMD)}$	DDR3 command buffer pull-down resistance	16	20	24	Ω	5
$R_{ON\_UP(CTL)}$	DDR3 control buffer pull-up resistance	16	20	23	Ω	5
$R_{ON\_DN(CTL)}$	DDR3 control buffer pull-down resistance	16	20	24	Ω	5
$V_{IL\_SM\_DRAMPWROK}$	Input Low Voltage for SM_DRAMPWROK	—	—	V_{DDQ} *.55 – 0.1	V	9
$V_{IH\_SM\_DRAMPWROK}$	Input High Voltage for SM_DRAMPWROK	V_{DDQ} *.55 +0.1	—	—	V	9
I_{LI}	Input Leakage Current (DQ, CK) 0 V 0.2*V_{DDQ} 0.8*V_{DDQ} V_{DDQ}	—	—	± 0.75 ± 0.55 ± 0.9 ± 1.4	mA	
I_{LI}	Input Leakage Current (CMD, CTL) 0 V 0.2*V_{DDQ} 0.8*V_{DDQ} V_{DDQ}	—	—	± 0.85 ± 0.65 ± 1.1 ± 1.65	mA	

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. V_{IL} is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
3. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
4. V_{IH} and V_{OH} may experience excursions above V_{DDQ}. However, input signal drivers must comply with the signal quality specifications.
5. This is the pull up/down driver resistance.
6. R_{TERM} is the termination on the DIMM and in not controlled by the processor.
7. The minimum and maximum values for these signals are programmable by BIOS to one of the two sets.
8. DDR3 values are pre-silicon estimations and subject to change.
9. SM_DRAMPWROK must have a maximum of 15 ns rise or fall time over V_{DDQ} * 0.55 ±200 mV and edge must be monotonic.

Table 7-9. Control Sideband and TAP Signal Group DC Specifications

Symbol	Parameter	Min	Max	Units	Notes^{1}
V_{IL}	Input Low Voltage	—	V_{CCIO} * 0.3	V	2
V_{IH}	Input High Voltage	V_{CCIO} * 0.7	—	V	2, 4
V_{OL}	Output Low Voltage	—	V_{CCIO} * 0.1	V	2
V_{OH}	Output High Voltage	V_{CCIO} * 0.9	—	V	2, 4
R_{ON}	Buffer on Resistance	23	73	Ω	
I_{LI}	Input Leakage Current	—	±200	µA	3

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The V_{CCIO} referred to in these specifications refers to instantaneous V_{CCIO}.
3. For V_{IN} between "0" V and V_{CCIO}. Measured when the driver is tristated.
4. V_{IH} and V_{OH} may experience excursions above V_{CCIO}. However, input signal drivers must comply with the signal quality specifications.

Table 7-10. PCI Express* DC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes^{1,11}
$V_{TX-DIFF-p-p\ Low}$	Low differential peak to peak Tx voltage swing	0.4	0.5	0.6	V	3
$V_{TX-DIFF-p-p}$	Differential peak to peak Tx voltage swing	0.8	1	1.2	V	3
$V_{TX\_CM-AC-p}$	Tx AC Peak Common Mode Output Voltage (Gen1 only)	—	—	20	mV	1, 2, 6
$V_{TX\_CM-AC-p-p}$	Tx AC Peak Common Mode Output Voltage (Gen2 only)	—	—	100	mV	1, 2
$Z_{TX-DIFF-DC}$	DC Differential Tx Impedance (Gen1 only)	80	90	120	Ω	1, 10
Z_{RX-DC}	DC Common Mode Rx Impedance	40	45	60	Ω	1, 8, 9
$Z_{RX-DIFF-DC}$	DC Differential Rx Impedance (Gen1 only)	80	90	120	Ω	1
$V_{RX-DIFFp-p}$	Differential Rx input Peak to Peak Voltage (Gen1 only)	0.175	—	1.2	V	1
$V_{RX-DIFFp-p}$	Differential Rx input Peak to Peak Voltage (Gen2 only)	0.12	—	1.2	V	1
$V_{RX\_CM-AC-p}$	Rx AC peak Common Mode Input Voltage	150	—	—	mV	1, 7
PEG_ICOMPO	Comp Resistance	24.75	25	25.25	Ω	4, 5
PEG_COMPI	Comp Resistance	24.75	25	25.25	Ω	4, 5
PEG_RCOMPO	Comp Resistance	24.75	25	25.25	Ω	4, 5

Notes:
1. Refer to the PCI Express Base Specification for more details.
2. $V_{TX-AC-CM-PP}$ and $V_{TX-AC-CM-P}$ are defined in the PCI Express Base Specification. Measurement is made over at least 10^^{6} UI.
3. As measured with compliance test load. Defined as 2*|V_{TXD+} − V_{TXD-} |.
4. COMP resistance must be provided on the system board with 1% resistors.
5. PEG_ICOMPO, PEG_COMPI, PEG_RCOMPO are the same resistor.
6. RMS value.
7. Measured at Rx pins into a pair of 50-Ω terminations into ground. Common mode peak voltage is defined by the expression: max{|(Vd+ - Vd-) - V-CMDC|}.
8. DC impedance limits are needed to ensure Receiver detect.
9. The Rx DC Common Mode Impedance must be present when the Receiver terminations are first enabled to ensure that the Receiver Detect occurs properly. Compensation of this impedance can start immediately and the 15 Rx Common Mode Impedance (constrained by RLRX-CM to 50 Ω ±20%) must be within the specified range by the time Detect is entered.
10. Low impedance defined during signaling. Parameter is captured for 5.0 GHz by RLTX-DIFF.
11. These are pre-silicon estimates and are subject to change.

7.11 Platform Environmental Control Interface (PECI) DC Specifications

PECI is an Intel proprietary interface that provides a communication channel between Intel processors and chipset components to external thermal monitoring devices. The processor contains a Digital Thermal Sensor (DTS) that reports a relative die temperature as an offset from Thermal Control Circuit (TCC) activation temperature. Temperature sensors located throughout the die are implemented as analog-to-digital converters calibrated at the factory. PECI provides an interface for external devices to read the DTS temperature for thermal management and fan speed control. More detailed information is provided in the *Platform Environment Control Interface (PECI) Specification*.

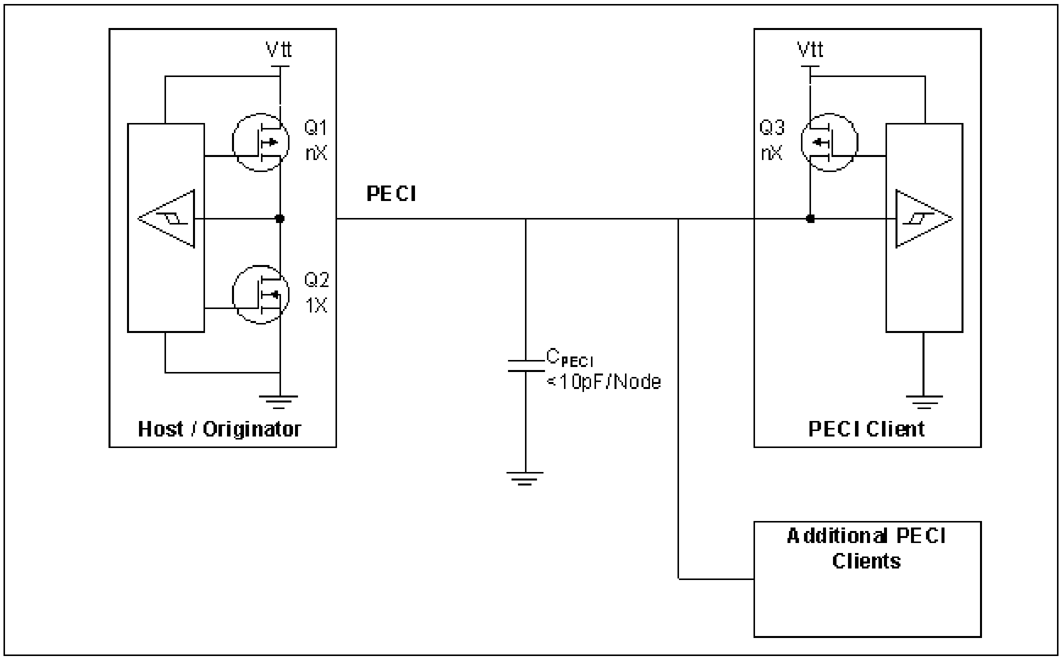
7.11.1 PECI Bus Architecture

The PECI architecture based on **wired OR bus** that the clients (as processor PECI) can pull up high (with strong drive).

The idle state on the bus is near zero.

Figure 7-1 demonstrates PECI design and connectivity, while the host/originator can be 3rd party PECI host, and one of the PECI clients is the processor PECI device.

Figure 7-1. Example for PECI Host-clients Connection



7.11.2 DC Characteristics

The PECI interface operates at a nominal voltage set by V_{CCIO}. The set of DC electrical specifications shown in Table 7-11 is used with devices normally operating from a V_{CCIO} interface supply. V_{CCIO} nominal levels will vary between processor families. All PECI devices will operate at the V_{CCIO} level determined by the processor installed in the system. For specific nominal V_{CCIO} levels, refer to Table 7-6.

Table 7-11. PECI DC Electrical Limits

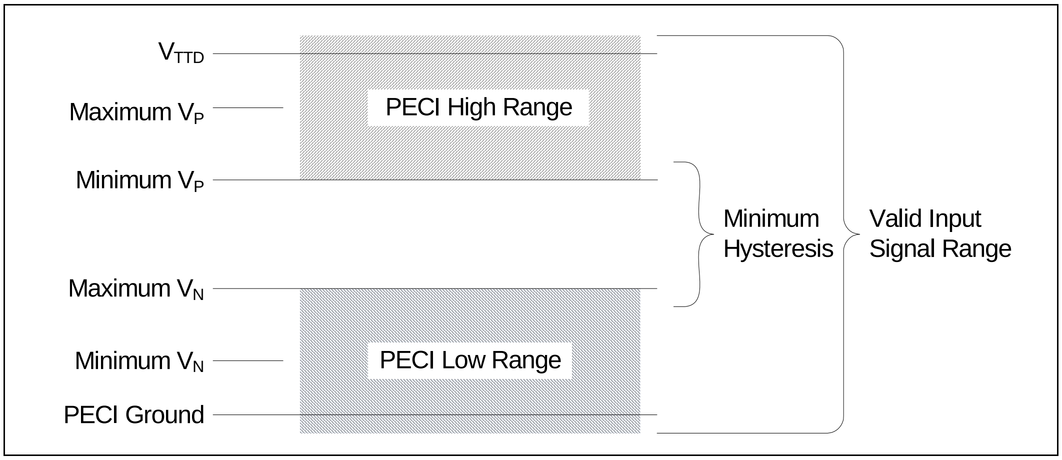
Symbol	Definition and Conditions	Min	Max	Units	Notes[1]
Rup	Internal pull up resistance	15	45	Ohm	3
V_{in}	Input Voltage Range	-0.15	V_{CCIO}	V	
$V_{hysteresis}$	Hysteresis	0.1 * V_{CCIO}	N/A	V	
V_n	Negative-Edge Threshold Voltage	0.275 * V_{CCIO}	0.500 * V_{CCIO}	V	
V_p	Positive-Edge Threshold Voltage	0.550 * V_{CCIO}	0.725 * V_{CCIO}	V	
C_{bus}	Bus Capacitance per Node	N/A	10	pF	
Cpad	Pad Capacitance	0.7	1.8	pF	
Ileak000	leakage current at 0V	—	0.6	mA	2
Ileak025	leakage current at 0.25*V_{CCIO}	—	0.4	mA	2
Ileak050	leakage current at 0.50*V_{CCIO}	—	0.2	mA	2
Ileak075	leakage current at 0.75*V_{CCIO}	—	0.13	mA	2
Ileak100	leakage current at V_{CCIO}	—	0.10	mA	2

Notes:
1. V_{CCIO} supplies the PECI interface. PECI behavior does not affect V_{CCIO} min/max specifications.
2. The leakage specification applies to powered devices on the PECI bus.
3. The PECI buffer internal pull up resistance measured at 0.75*V_{CCIO}

7.11.3 Input Device Hysteresis

The input buffers in both client and host models must use a Schmitt-triggered input design for improved noise immunity. Use Figure 7-2 as a guide for input buffer design.

Figure 7-2. Input Device Hysteresis



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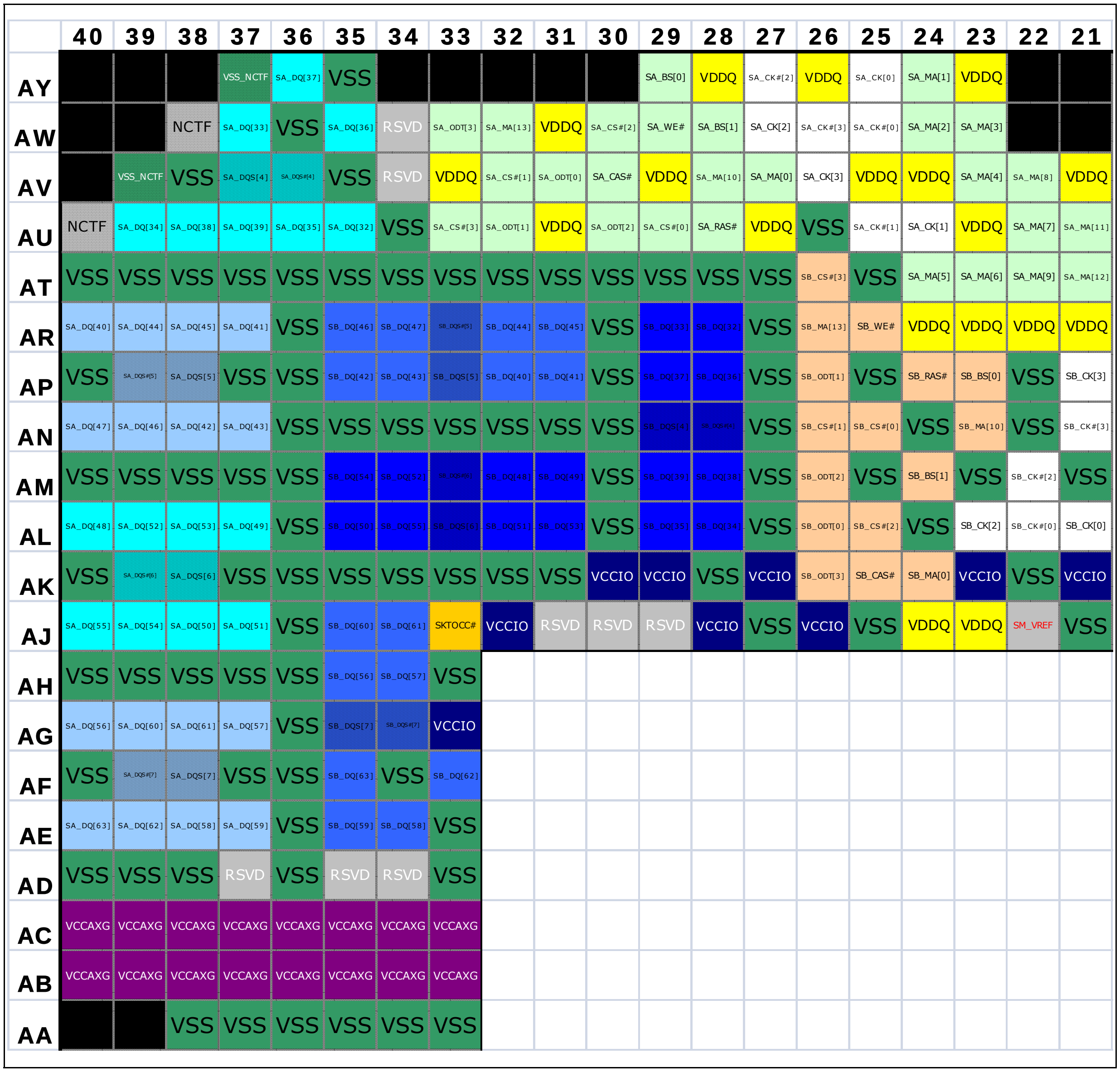
8 Processor Pin and Signal Information

8.1 Processor Pin Assignments

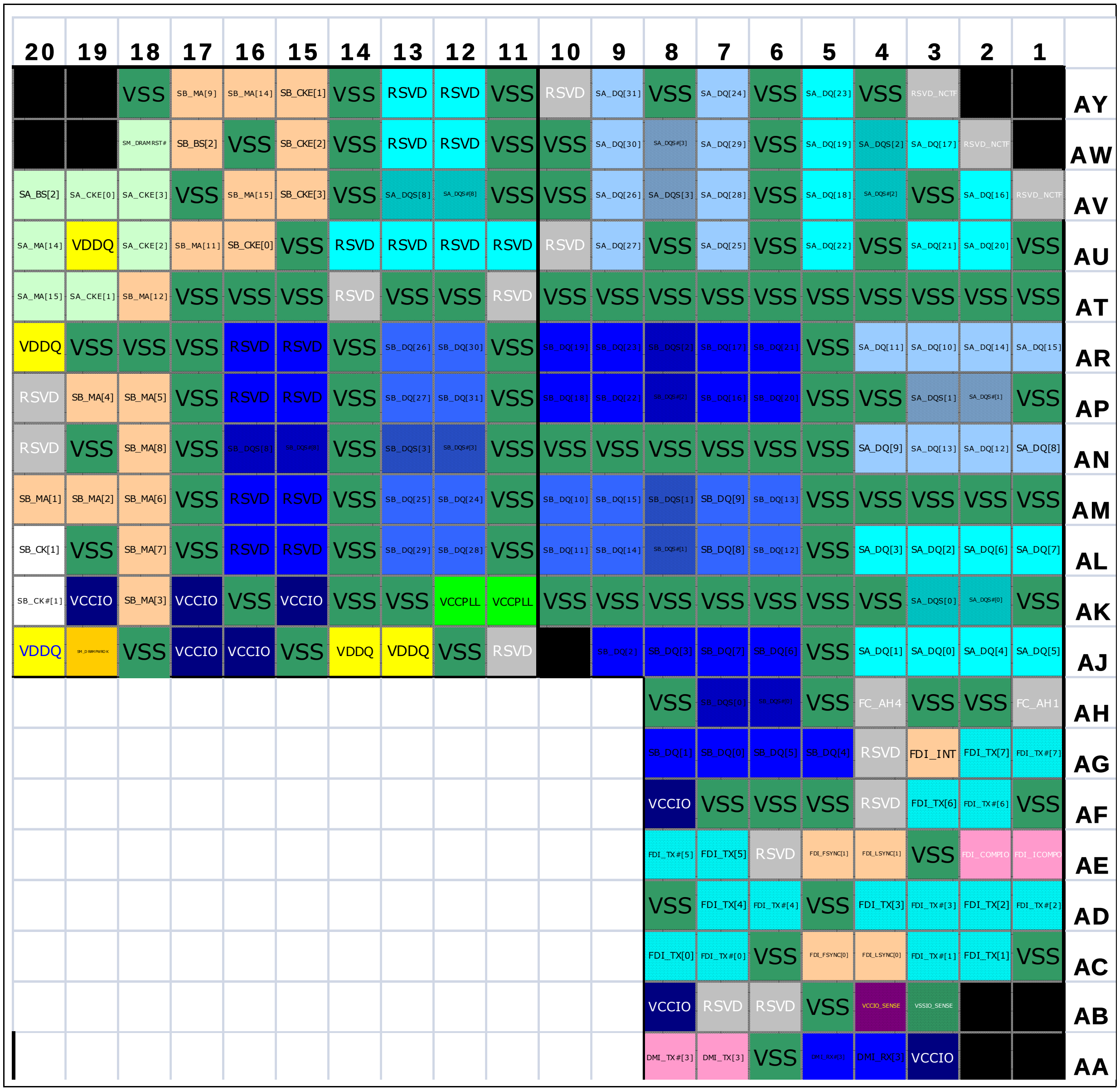
The processor pinmap quadrants are shown in Figure 8-1 through Figure 8-4. Table 8-1 provides a listing of all processor pins ordered alphabetically by pin name.

Figure 8-1. Socket Pinmap (Top View, Upper-Left Quadrant)



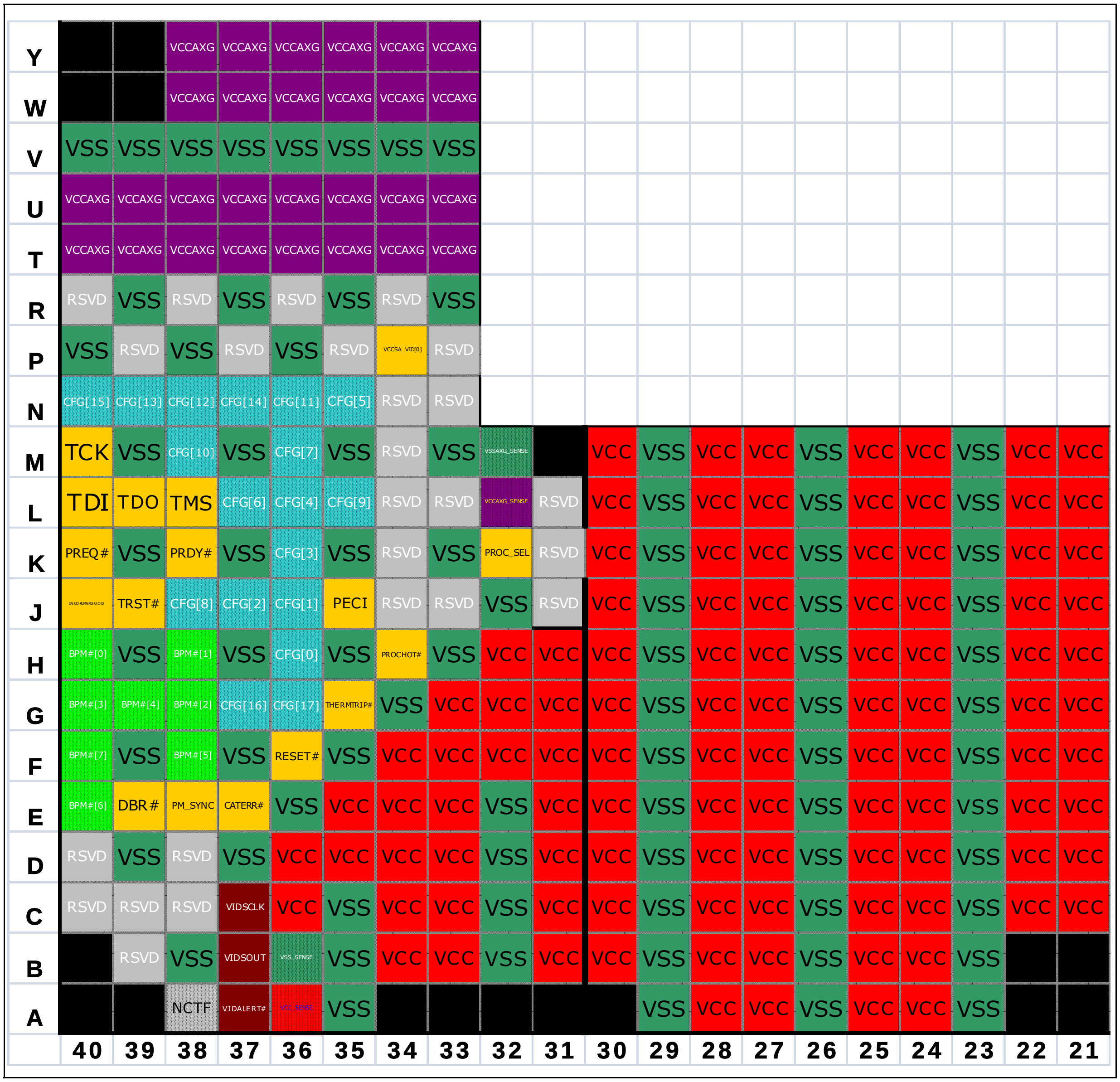
	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21
AY				VSS_NCTF	SA_DQ[37]	VSS						SA_BS[0]	VDDQ	SA_CK#[2]	VDDQ	SA_CK[0]	SA_MA[1]	VDDQ		
AW			NCTF	SA_DQ[33]	VSS	SA_DQ[36]	RSVD	SA_ODT[3]	SA_MA[13]	VDDQ	SA_CS#[2]	SA_WE#	SA_BS[1]	SA_CK[2]	SA_CK#[3]	SA_CK#[0]	SA_MA[2]	SA_MA[3]		
AV		VSS_NCTF	VSS	SA_DQS[4]	SA_DQS#[4]	VSS	RSVD	VDDQ	SA_CS#[1]	SA_ODT[0]	SA_CAS#	VDDQ	SA_MA[10]	SA_MA[0]	SA_CK[3]	VDDQ	VDDQ	SA_MA[4]	SA_MA[8]	VDDQ
AU	NCTF	SA_DQ[34]	SA_DQ[38]	SA_DQ[39]	SA_DQ[35]	SA_DQ[32]	VSS	SA_CS#[3]	SA_ODT[1]	VDDQ	SA_ODT[2]	SA_CS#[0]	SA_RAS#	VDDQ	VSS	SA_CK#[1]	SA_CK[1]	VDDQ	SA_MA[7]	SA_MA[11]
AT	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	SB_CS#[3]	VSS	SA_MA[5]	SA_MA[6]	SA_MA[9]	SA_MA[12]
AR	SA_DQ[40]	SA_DQ[44]	SA_DQ[45]	SA_DQ[41]	VSS	SB_DQ[46]	SB_DQ[47]	SB_DQS#[5]	SB_DQ[44]	SB_DQ[45]	VSS	SB_DQ[33]	SB_DQ[32]	VSS	SB_MA[13]	SB_WE#	VDDQ	VDDQ	VDDQ	VDDQ
AP	VSS	SA_DQS#[5]	SA_DQS[5]	VSS	VSS	SB_DQ[42]	SB_DQ[43]	SB_DQS[5]	SB_DQ[40]	SB_DQ[41]	VSS	SB_DQ[37]	SB_DQ[36]	VSS	SB_ODT[1]	VSS	SB_RAS#	SB_BS[0]	VSS	SB_CK[3]
AN	SA_DQ[47]	SA_DQ[46]	SA_DQ[42]	SA_DQ[43]	VSS	VSS	VSS	VSS	VSS	VSS	VSS	SB_DQS[4]	SB_DQS#[4]	VSS	SB_CS#[1]	SB_CS#[0]	VSS	SB_MA[10]	VSS	SB_CK#[3]
AM	VSS	VSS	VSS	VSS	VSS	SB_DQ[54]	SB_DQ[52]	SB_DQS#[6]	SB_DQ[48]	SB_DQ[49]	VSS	SB_DQ[39]	SB_DQ[38]	VSS	SB_ODT[2]	VSS	SB_BS[1]	VSS	SB_CK#[2]	VSS
AL	SA_DQ[48]	SA_DQ[52]	SA_DQ[53]	SA_DQ[49]	VSS	SB_DQ[50]	SB_DQ[55]	SB_DQS[6]	SB_DQ[51]	SB_DQ[53]	VSS	SB_DQ[35]	SB_DQ[34]	VSS	SB_ODT[0]	SB_CS#[2]	VSS	SB_CK[2]	SB_CK#[0]	SB_CK[0]
AK	VSS	SA_DQS#[6]	SA_DQS[6]	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCCIO	VCCIO	VSS	VCCIO	SB_ODT[3]	SB_CAS#	SB_MA[0]	VCCIO	VSS	VCCIO
AJ	SA_DQ[55]	SA_DQ[54]	SA_DQ[50]	SA_DQ[51]	VSS	SB_DQ[60]	SB_DQ[61]	SKTOCC#	VCCIO	RSVD	RSVD	RSVD	VCCIO	VSS	VCCIO	VSS	VDDQ	VDDQ	SM_VREF	VSS
AH	VSS	VSS	VSS	VSS	VSS	SB_DQ[56]	SB_DQ[57]	VSS												
AG	SA_DQ[56]	SA_DQ[60]	SA_DQ[61]	SA_DQ[57]	VSS	SB_DQS[7]	SB_DQS#[7]	VCCIO												
AF	VSS	SA_DQS#[7]	SA_DQS[7]	VSS	VSS	SB_DQ[63]	VSS	SB_DQ[62]												
AE	SA_DQ[63]	SA_DQ[62]	SA_DQ[58]	SA_DQ[59]	VSS	SB_DQ[59]	SB_DQ[58]	VSS												
AD	VSS	VSS	VSS	RSVD	VSS	RSVD	RSVD	VSS												
AC	VCCAXG	VCCAXG	VCCAXG	VCCAXG	VCCAXG	VCCAXG	VCCAXG	VCCAXG												
AB	VCCAXG	VCCAXG	VCCAXG	VCCAXG	VCCAXG	VCCAXG	VCCAXG	VCCAXG												
AA			VSS	VSS	VSS	VSS	VSS	VSS												

Figure 8-2. Socket Pinmap (Top View, Upper-Right Quadrant)



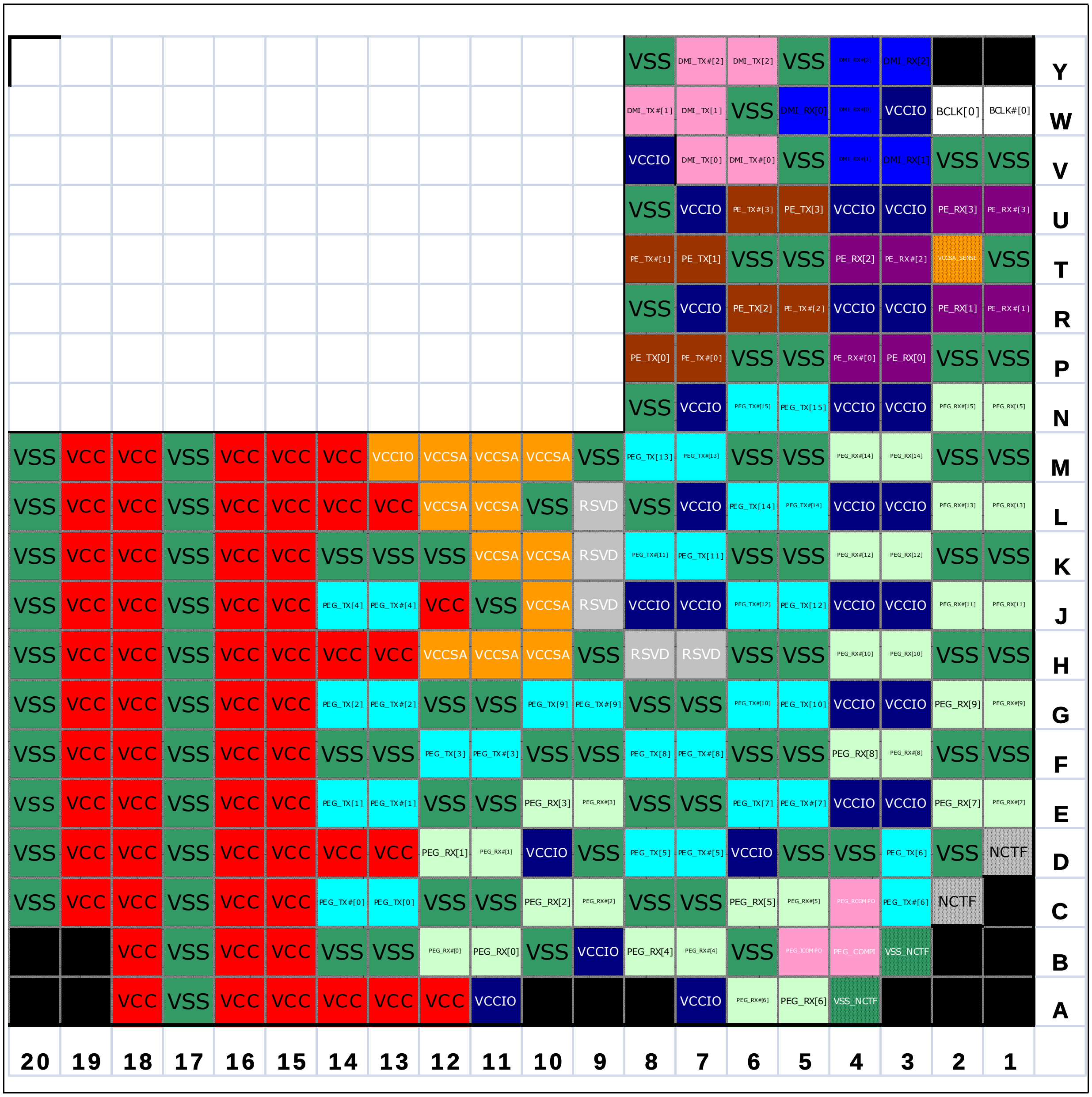
20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
		VSS	SB_MA[9]	SB_MA[14]	SB_CKE[1]	VSS	RSVD	RSVD	VSS	RSVD	SA_DQ[31]	VSS	SA_DQ[24]	VSS	SA_DQ[23]	VSS	RSVD_NCTF			AY
		SM_DRAMRST#	SB_BS[2]	VSS	SB_CKE[2]	VSS	RSVD	RSVD	VSS	VSS	SA_DQ[30]	SA_DQS#[3]	SA_DQ[29]	VSS	SA_DQ[19]	SA_DQS[2]	SA_DQ[17]	RSVD_NCTF		AW
SA_BS[2]	SA_CKE[0]	SA_CKE[3]	VSS	SB_MA[15]	SB_CKE[3]	VSS	SA_DQS[8]	SA_DQS#[8]	VSS	VSS	SA_DQ[26]	SA_DQS[3]	SA_DQ[28]	VSS	SA_DQ[18]	SA_DQS#[2]	VSS	SA_DQ[16]	RSVD_NCTF	AV
SA_MA[14]	VDDQ	SA_CKE[2]	SB_MA[11]	SB_CKE[0]	VSS	RSVD	RSVD	RSVD	RSVD	RSVD	SA_DQ[27]	VSS	SA_DQ[25]	VSS	SA_DQ[22]	VSS	SA_DQ[21]	SA_DQ[20]	VSS	AU
SA_MA[15]	SA_CKE[1]	SB_MA[12]	VSS	VSS	VSS	RSVD	VSS	VSS	RSVD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	AT
VDDQ	VSS	VSS	VSS	RSVD	RSVD	VSS	SB_DQ[26]	SB_DQ[30]	VSS	SB_DQ[19]	SB_DQ[23]	SB_DQS[2]	SB_DQ[17]	SB_DQ[21]	VSS	SA_DQ[11]	SA_DQ[10]	SA_DQ[14]	SA_DQ[15]	AR
RSVD	SB_MA[4]	SB_MA[5]	VSS	RSVD	RSVD	VSS	SB_DQ[27]	SB_DQ[31]	VSS	SB_DQ[18]	SB_DQ[22]	SB_DQS#[2]	SB_DQ[16]	SB_DQ[20]	VSS	VSS	SA_DQS[1]	SA_DQS#[1]	VSS	AP
RSVD	VSS	SB_MA[8]	VSS	SB_DQS[8]	SB_DQS#[8]	VSS	SB_DQS[3]	SB_DQS#[3]	VSS	VSS	VSS	VSS	VSS	VSS	VSS	SA_DQ[9]	SA_DQ[13]	SA_DQ[12]	SA_DQ[8]	AN
SB_MA[1]	SB_MA[2]	SB_MA[6]	VSS	RSVD	RSVD	VSS	SB_DQ[25]	SB_DQ[24]	VSS	SB_DQ[10]	SB_DQ[15]	SB_DQS[1]	SB_DQ[9]	SB_DQ[13]	VSS	VSS	VSS	VSS	VSS	AM
SB_CK[1]	VSS	SB_MA[7]	VSS	RSVD	RSVD	VSS	SB_DQ[29]	SB_DQ[28]	VSS	SB_DQ[11]	SB_DQ[14]	SB_DQS#[1]	SB_DQ[8]	SB_DQ[12]	VSS	SA_DQ[3]	SA_DQ[2]	SA_DQ[6]	SA_DQ[7]	AL
SB_CK#[1]	VCCIO	SB_MA[3]	VCCIO	VSS	VCCIO	VSS	VSS	VCCPLL	VCCPLL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	SA_DQS[0]	SA_DQS#[0]	VSS	AK
VDDQ	SM_DRAMPWROK	VSS	VCCIO	VCCIO	VSS	VDDQ	VDDQ	VSS	RSVD		SB_DQ[2]	SB_DQ[3]	SB_DQ[7]	SB_DQ[6]	VSS	SA_DQ[1]	SA_DQ[0]	SA_DQ[4]	SA_DQ[5]	AJ
												VSS	SB_DQS[0]	SB_DQS#[0]	VSS	FC_AH4	VSS	VSS	FC_AH1	AH
												SB_DQ[1]	SB_DQ[0]	SB_DQ[5]	SB_DQ[4]	RSVD	FDI_INT	FDI_TX[7]	FDI_TX#[7]	AG
												VCCIO	VSS	VSS	VSS	RSVD	FDI_TX[6]	FDI_TX#[6]	VSS	AF
												FDI_TX#[5]	FDI_TX[5]	RSVD	FDI_FSYNC[1]	FDI_LSYNC[1]	VSS	FDI_COMPIO	FDI_ICOMPO	AE
												VSS	FDI_TX[4]	FDI_TX#[4]	VSS	FDI_TX[3]	FDI_TX#[3]	FDI_TX[2]	FDI_TX#[2]	AD
												FDI_TX[0]	FDI_TX#[0]	VSS	FDI_FSYNC[0]	FDI_LSYNC[0]	FDI_TX#[1]	FDI_TX[1]	VSS	AC
												VCCIO	RSVD	RSVD	VSS	VCCIO_SENSE	VSSIO_SENSE			AB
												DMI_TX#[3]	DMI_TX[3]	VSS	DMI_RX#[3]	DMI_RX[3]	VCCIO			AA

Figure 8-3. Socket Pinmap (Top View, Lower-Left Quadrant)



Y			VCCAXG	VCCAXG	VCCAXG	VCCAXG	VCCAXG	VCCAXG												
W			VCCAXG	VCCAXG	VCCAXG	VCCAXG	VCCAXG	VCCAXG												
V	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS												
U	VCCAXG	VCCAXG	VCCAXG	VCCAXG	VCCAXG	VCCAXG	VCCAXG	VCCAXG												
T	VCCAXG	VCCAXG	VCCAXG	VCCAXG	VCCAXG	VCCAXG	VCCAXG	VCCAXG												
R	RSVD	VSS	RSVD	VSS	RSVD	VSS	RSVD	VSS												
P	VSS	RSVD	VSS	RSVD	VSS	RSVD	VCCSA_VID[0]	RSVD												
N	CFG[15]	CFG[13]	CFG[12]	CFG[14]	CFG[11]	CFG[5]	RSVD	RSVD												
M	TCK	VSS	CFG[10]	VSS	CFG[7]	VSS	RSVD	VSS	VSSAXG_SENSE		VCC	VSS	VCC	VCC	VSS	VCC	VCC	VSS	VCC	VCC
L	TDI	TDO	TMS	CFG[6]	CFG[4]	CFG[9]	RSVD	RSVD	VCCAXG_SENSE	RSVD	VCC	VSS	VCC	VCC	VSS	VCC	VCC	VSS	VCC	VCC
K	PREQ#	VSS	PRDY#	VSS	CFG[3]	VSS	RSVD	VSS	PROC_SEL	RSVD	VCC	VSS	VCC	VCC	VSS	VCC	VCC	VSS	VCC	VCC
J	UNCOREPWRGOOD	TRST#	CFG[8]	CFG[2]	CFG[1]	PECI	RSVD	RSVD	VSS	RSVD	VCC	VSS	VCC	VCC	VSS	VCC	VCC	VSS	VCC	VCC
H	BPM#[0]	VSS	BPM#[1]	VSS	CFG[0]	VSS	PROCHOT#	VSS	VCC	VCC	VCC	VSS	VCC	VCC	VSS	VCC	VCC	VSS	VCC	VCC
G	BPM#[3]	BPM#[4]	BPM#[2]	CFG[16]	CFG[17]	THERMTRIP#	VSS	VCC	VCC	VCC	VCC	VSS	VCC	VCC	VSS	VCC	VCC	VSS	VCC	VCC
F	BPM#[7]	VSS	BPM#[5]	VSS	RESET#	VSS	VCC	VCC	VCC	VCC	VCC	VSS	VCC	VCC	VSS	VCC	VCC	VSS	VCC	VCC
E	BPM#[6]	DBR#	PM_SYNC	CATERR#	VSS	VCC	VCC	VCC	VSS	VCC	VCC	VSS	VCC	VCC	VSS	VCC	VCC	VSS	VCC	VCC
D	RSVD	VSS	RSVD	VSS	VCC	VCC	VCC	VCC	VSS	VCC	VCC	VSS	VCC	VCC	VSS	VCC	VCC	VSS	VCC	VCC
C	RSVD	RSVD	RSVD	VIDSCLK	VCC	VSS	VCC	VCC	VSS	VCC	VCC	VSS	VCC	VCC	VSS	VCC	VCC	VSS	VCC	VCC
B		RSVD	VSS	VIDSOUT	VSS_SENSE	VSS	VCC	VCC	VSS	VCC	VCC	VSS	VCC	VCC	VSS	VCC	VCC	VSS		
A			NCTF	VIDALERT#	VCC_SENSE	VSS						VSS	VCC	VCC	VSS	VCC	VCC	VSS		
	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21

Figure 8-4. Socket Pinmap (Top View, Lower-Right Quadrant)



												VSS	DMI_TX#[2]	DMI_TX[2]	VSS	DMI_RX#[2]	DMI_RX[2]			**Y**
												DMI_TX#[1]	DMI_TX[1]	VSS	DMI_RX[0]	DMI_RX#[0]	VCCIO	BCLK[0]	BCLK#[0]	**W**
												VCCIO	DMI_TX[0]	DMI_TX#[0]	VSS	DMI_RX#[1]	DMI_RX[1]	VSS	VSS	**V**
												VSS	VCCIO	PE_TX#[3]	PE_TX[3]	VCCIO	VCCIO	PE_RX[3]	PE_RX#[3]	**U**
												PE_TX#[1]	PE_TX[1]	VSS	VSS	PE_RX[2]	PE_RX#[2]	VCCSA_SENSE	VSS	**T**
												VSS	VCCIO	PE_TX[2]	PE_TX#[2]	VCCIO	VCCIO	PE_RX[1]	PE_RX#[1]	**R**
												PE_TX[0]	PE_TX#[0]	VSS	VSS	PE_RX#[0]	PE_RX[0]	VSS	VSS	**P**
												VSS	VCCIO	PEG_TX#[15]	PEG_TX[15]	VCCIO	VCCIO	PEG_RX#[15]	PEG_RX[15]	**N**
VSS	VCC	VCC	VSS	VCC	VCC	VCC	VCCIO	VCCSA	VCCSA	VCCSA	VSS	PEG_TX[13]	PEG_TX#[13]	VSS	VSS	PEG_RX#[14]	PEG_RX[14]	VSS	VSS	**M**
VSS	VCC	VCC	VSS	VCC	VCC	VCC	VCC	VCCSA	VCCSA	VSS	RSVD	VSS	VCCIO	PEG_TX[14]	PEG_TX#[14]	VCCIO	VCCIO	PEG_RX#[13]	PEG_RX[13]	**L**
VSS	VCC	VCC	VSS	VCC	VCC	VSS	VSS	VSS	VCCSA	VCCSA	RSVD	PEG_TX#[11]	PEG_TX[11]	VSS	VSS	PEG_RX#[12]	PEG_RX[12]	VSS	VSS	**K**
VSS	VCC	VCC	VSS	VCC	VCC	PEG_TX[4]	PEG_TX#[4]	VCC	VSS	VCCSA	RSVD	VCCIO	VCCIO	PEG_TX#[12]	PEG_TX[12]	VCCIO	VCCIO	PEG_RX#[11]	PEG_RX[11]	**J**
VSS	VCC	VCC	VSS	VCC	VCC	VCC	VCC	VCCSA	VCCSA	VCCSA	VSS	RSVD	RSVD	VSS	VSS	PEG_RX#[10]	PEG_RX[10]	VSS	VSS	**H**
VSS	VCC	VCC	VSS	VCC	VCC	PEG_TX[2]	PEG_TX#[2]	VSS	VSS	PEG_TX[9]	PEG_TX#[9]	VSS	VSS	PEG_TX#[10]	PEG_TX[10]	VCCIO	VCCIO	PEG_RX[9]	PEG_RX#[9]	**G**
VSS	VCC	VCC	VSS	VCC	VCC	VSS	VSS	PEG_TX[3]	PEG_TX#[3]	VSS	VSS	PEG_TX[8]	PEG_TX#[8]	VSS	VSS	PEG_RX[8]	PEG_RX#[8]	VSS	VSS	**F**
VSS	VCC	VCC	VSS	VCC	VCC	PEG_TX[1]	PEG_TX#[1]	VSS	VSS	PEG_RX[3]	PEG_RX#[3]	VSS	VSS	PEG_TX[7]	PEG_TX#[7]	VCCIO	VCCIO	PEG_RX[7]	PEG_RX#[7]	**E**
VSS	VCC	VCC	VSS	VCC	VCC	VCC	VCC	PEG_RX[1]	PEG_RX#[1]	VCCIO	VSS	PEG_TX[5]	PEG_TX#[5]	VCCIO	VSS	VSS	PEG_TX[6]	VSS	NCTF	**D**
VSS	VCC	VCC	VSS	VCC	VCC	PEG_TX#[0]	PEG_TX[0]	VSS	VSS	PEG_RX[2]	PEG_RX#[2]	VSS	VSS	PEG_RX[5]	PEG_RX#[5]	PEG_RCOMPO	PEG_TX#[6]	NCTF		**C**
		VCC	VSS	VCC	VCC	VSS	VSS	PEG_RX#[0]	PEG_RX[0]	VSS	VCCIO	PEG_RX[4]	PEG_RX#[4]	VSS	PEG_ICOMPO	PEG_COMPI	VSS_NCTF			**B**
		VCC	VSS	VCC	VCC	VCC	VCC	VCC	VCCIO				VCCIO	PEG_RX#[6]	PEG_RX[6]	VSS_NCTF				**A**
20	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	

Table 8-1. Processor Pin List by Pin Name

Pin Name	Pin #	Buffer Type	Dir.
BCLK_ITP	C40	Diff Clk	I
BCLK_ITP#	D40	Diff Clk	I
BCLK[0]	W2	Diff Clk	I
BCLK#[0]	W1	Diff Clk	I
BPM#[0]	H40	GTL	I/O
BPM#[1]	H38	GTL	I/O
BPM#[2]	G38	GTL	I/O
BPM#[3]	G40	GTL	I/O
BPM#[4]	G39	GTL	I/O
BPM#[5]	F38	GTL	I/O
BPM#[6]	E40	GTL	I/O
BPM#[7]	F40	GTL	I/O
CATERR#	E37	GTL	O
CFG[0]	H36	CMOS	I
CFG[1]	J36	CMOS	I
CFG[10]	M38	CMOS	I
CFG[11]	N36	CMOS	I
CFG[12]	N38	CMOS	I
CFG[13]	N39	CMOS	I
CFG[14]	N37	CMOS	I
CFG[15]	N40	CMOS	I
CFG[16]	G37	CMOS	I
CFG[17]	G36	CMOS	I
CFG[2]	J37	CMOS	I
CFG[3]	K36	CMOS	I
CFG[4]	L36	CMOS	I
CFG[5]	N35	CMOS	I
CFG[6]	L37	CMOS	I
CFG[7]	M36	CMOS	I
CFG[8]	J38	CMOS	I
CFG[9]	L35	CMOS	I
DBR#	E39	Async CMOS	O
DMI_RX[0]	W5	DMI	I
DMI_RX[1]	V3	DMI	I
DMI_RX[2]	Y3	DMI	I
DMI_RX[3]	AA4	DMI	I
DMI_RX#[0]	W4	DMI	I
DMI_RX#[1]	V4	DMI	I
DMI_RX#[2]	Y4	DMI	I
DMI_RX#[3]	AA5	DMI	I
DMI_TX[0]	V7	DMI	O
DMI_TX[1]	W7	DMI	O
DMI_TX[2]	Y6	DMI	O
DMI_TX[3]	AA7	DMI	O
DMI_TX#[0]	V6	DMI	O
DMI_TX#[1]	W8	DMI	O
DMI_TX#[2]	Y7	DMI	O
DMI_TX#[3]	AA8	DMI	O
FC_AH1	AH1	N/A	O
FC_AH4	AH4	N/A	O
FDI_COMPIO	AE2	Analog	I
FDI_FSYNC[0]	AC5	CMOS	I
FDI_FSYNC[1]	AE5	CMOS	I
FDI_ICOMPO	AE1	Analog	I
FDI_INT	AG3	CMOS	I
FDI_LSYNC[0]	AC4	CMOS	I
FDI_LSYNC[1]	AE4	CMOS	I
FDI_TX[0]	AC8	FDI	O
FDI_TX[1]	AC2	FDI	O
FDI_TX[2]	AD2	FDI	O
FDI_TX[3]	AD4	FDI	O
FDI_TX[4]	AD7	FDI	O
FDI_TX[5]	AE7	FDI	O
FDI_TX[6]	AF3	FDI	O
FDI_TX[7]	AG2	FDI	O
FDI_TX#[0]	AC7	FDI	O
FDI_TX#[1]	AC3	FDI	O
FDI_TX#[2]	AD1	FDI	O
FDI_TX#[3]	AD3	FDI	O
FDI_TX#[4]	AD6	FDI	O
FDI_TX#[5]	AE8	FDI	O
FDI_TX#[6]	AF2	FDI	O
FDI_TX#[7]	AG1	FDI	O
NCTF	A38		
NCTF	AU40		
NCTF	AW38		
NCTF	C2		
NCTF	D1		
PE_RX[0]	P3	PCI Express	I
PE_RX[1]	R2	PCI Express	I
PE_RX[2]	T4	PCI Express	I
PE_RX[3]	U2	PCI Express	I
PE_RX#[0]	P4	PCI Express	I
PE_RX#[1]	R1	PCI Express	I
PE_RX#[2]	T3	PCI Express	I
PE_RX#[3]	U1	PCI Express	I
PE_TX[0]	P8	PCI Express	O
PE_TX[1]	T7	PCI Express	O

Table 8-1. Processor Pin List by Pin Name

Pin Name	Pin #	Buffer Type	Dir.
PE_TX[2]	R6	PCI Express	O
PE_TX[3]	U5	PCI Express	O
PE_TX#[0]	P7	PCI Express	O
PE_TX#[1]	T8	PCI Express	O
PE_TX#[2]	R5	PCI Express	O
PE_TX#[3]	U6	PCI Express	O
PECI	J35	Async	I/O
PEG_COMPI	B4	Analog	I
PEG_ICOMPO	B5	Analog	I
PEG_RCOMPO	C4	Analog	I
PEG_RX[0]	B11	PCI Express	I
PEG_RX[1]	D12	PCI Express	I
PEG_RX[10]	H3	PCI Express	I
PEG_RX[11]	J1	PCI Express	I
PEG_RX[12]	K3	PCI Express	I
PEG_RX[13]	L1	PCI Express	I
PEG_RX[14]	M3	PCI Express	I
PEG_RX[15]	N1	PCI Express	I
PEG_RX[2]	C10	PCI Express	I
PEG_RX[3]	E10	PCI Express	I
PEG_RX[4]	B8	PCI Express	I
PEG_RX[5]	C6	PCI Express	I
PEG_RX[6]	A5	PCI Express	I
PEG_RX[7]	E2	PCI Express	I
PEG_RX[8]	F4	PCI Express	I
PEG_RX[9]	G2	PCI Express	I
PEG_RX#[0]	B12	PCI Express	I
PEG_RX#[1]	D11	PCI Express	I
PEG_RX#[10]	H4	PCI Express	I
PEG_RX#[11]	J2	PCI Express	I
PEG_RX#[12]	K4	PCI Express	I
PEG_RX#[13]	L2	PCI Express	I
PEG_RX#[14]	M4	PCI Express	I
PEG_RX#[15]	N2	PCI Express	I
PEG_RX#[2]	C9	PCI Express	I
PEG_RX#[3]	E9	PCI Express	I
PEG_RX#[4]	B7	PCI Express	I
PEG_RX#[5]	C5	PCI Express	I
PEG_RX#[6]	A6	PCI Express	I
PEG_RX#[7]	E1	PCI Express	I
PEG_RX#[8]	F3	PCI Express	I
PEG_RX#[9]	G1	PCI Express	I
PEG_TX[0]	C13	PCI Express	O
PEG_TX[1]	E14	PCI Express	O
PEG_TX[2]	G14	PCI Express	O
PEG_TX[3]	F12	PCI Express	O
PEG_TX[4]	J14	PCI Express	O
PEG_TX[5]	D8	PCI Express	O
PEG_TX[6]	D3	PCI Express	O
PEG_TX[7]	E6	PCI Express	O
PEG_TX[8]	F8	PCI Express	O
PEG_TX[9]	G10	PCI Express	O
PEG_TX[10]	G5	PCI Express	O
PEG_TX[11]	K7	PCI Express	O
PEG_TX[12]	J5	PCI Express	O
PEG_TX[13]	M8	PCI Express	O
PEG_TX[14]	L6	PCI Express	O
PEG_TX[15]	N5	PCI Express	O
PEG_TX#[0]	C14	PCI Express	O
PEG_TX#[1]	E13	PCI Express	O
PEG_TX#[2]	G13	PCI Express	O
PEG_TX#[3]	F11	PCI Express	O
PEG_TX#[4]	J13	PCI Express	O
PEG_TX#[5]	D7	PCI Express	O
PEG_TX#[6]	C3	PCI Express	O
PEG_TX#[7]	E5	PCI Express	O
PEG_TX#[8]	F7	PCI Express	O
PEG_TX#[9]	G9	PCI Express	O
PEG_TX#[10]	G6	PCI Express	O
PEG_TX#[11]	K8	PCI Express	O
PEG_TX#[12]	J6	PCI Express	O
PEG_TX#[13]	M7	PCI Express	O
PEG_TX#[14]	L5	PCI Express	O
PEG_TX#[15]	N6	PCI Express	O
PM_SYNC	E38	CMOS	I
PRDY#	K38	Async GTL	O
PREQ#	K40	Async GTL	I
PROC_SEL	K32	N/A	O
PROCHOT#	H34	Async GTL	I/O
RESET#	F36	CMOS	I
RSVD	AB6		
RSVD	AB7		
RSVD	AD37		
RSVD	AE6		
RSVD	AF4		
RSVD	AG4		
RSVD	AJ11		
RSVD	AJ29		

Table 8-1. Processor Pin List by Pin Name

Pin Name	Pin #	Buffer Type	Dir.
RSVD	AJ30		
RSVD	AJ31		
RSVD	AN20		
RSVD	AP20		
RSVD	AT11		
RSVD	AT14		
RSVD	AU10		
RSVD	AV34		
RSVD	AW34		
RSVD	AY10		
RSVD	C38		
RSVD	C39		
RSVD	D38		
RSVD	H7		
RSVD	H8		
RSVD	J33		
RSVD	J34		
RSVD	J9		
RSVD	K34		
RSVD	K9		
RSVD	L31		
RSVD	L33		
RSVD	L34		
RSVD	L9		
RSVD	M34		
RSVD	N33		
RSVD	N34		
RSVD	P35		
RSVD	P37		
RSVD	P39		
RSVD	R34		
RSVD	R36		
RSVD	R38		
RSVD	R40		
RSVD	J31		
RSVD	AD34		
RSVD	AD35		
RSVD	K31		
RSVD_NCTF	AV1		
RSVD_NCTF	AW2		
RSVD_NCTF	AY3		
RSVD_NCTF	B39		
SA_BS[0]	AY29	DDR3	O
SA_BS[1]	AW28	DDR3	O
SA_BS[2]	AV20	DDR3	O
SA_CAS#	AV30	DDR3	O
SA_CK[0]	AY25	DDR3	O
SA_CK[1]	AU24	DDR3	O
SA_CK[2]	AW27	DDR3	O
SA_CK[3]	AV26	DDR3	O
SA_CK#[0]	AW25	DDR3	O
SA_CK#[1]	AU25	DDR3	O
SA_CK#[2]	AY27	DDR3	O
SA_CK#[3]	AW26	DDR3	O
SA_CKE[0]	AV19	DDR3	O
SA_CKE[1]	AT19	DDR3	O
SA_CKE[2]	AU18	DDR3	O
SA_CKE[3]	AV18	DDR3	O
SA_CS#[0]	AU29	DDR3	O
SA_CS#[1]	AV32	DDR3	O
SA_CS#[2]	AW30	DDR3	O
SA_CS#[3]	AU33	DDR3	O
SA_DQ[0]	AJ3	DDR3	I/O
SA_DQ[1]	AJ4	DDR3	I/O
SA_DQ[2]	AL3	DDR3	I/O
SA_DQ[3]	AL4	DDR3	I/O
SA_DQ[4]	AJ2	DDR3	I/O
SA_DQ[5]	AJ1	DDR3	I/O
SA_DQ[6]	AL2	DDR3	I/O
SA_DQ[7]	AL1	DDR3	I/O
SA_DQ[8]	AN1	DDR3	I/O
SA_DQ[9]	AN4	DDR3	I/O
SA_DQ[10]	AR3	DDR3	I/O
SA_DQ[11]	AR4	DDR3	I/O
SA_DQ[12]	AN2	DDR3	I/O
SA_DQ[13]	AN3	DDR3	I/O
SA_DQ[14]	AR2	DDR3	I/O
SA_DQ[15]	AR1	DDR3	I/O
SA_DQ[16]	AV2	DDR3	I/O
SA_DQ[17]	AW3	DDR3	I/O
SA_DQ[18]	AV5	DDR3	I/O
SA_DQ[19]	AW5	DDR3	I/O
SA_DQ[20]	AU2	DDR3	I/O
SA_DQ[21]	AU3	DDR3	I/O
SA_DQ[22]	AU5	DDR3	I/O
SA_DQ[23]	AY5	DDR3	I/O
SA_DQ[24]	AY7	DDR3	I/O
SA_DQ[25]	AU7	DDR3	I/O

Table 8-1. Processor Pin List by Pin Name

Pin Name	Pin #	Buffer Type	Dir.
SA_DQ[26]	AV9	DDR3	I/O
SA_DQ[27]	AU9	DDR3	I/O
SA_DQ[28]	AV7	DDR3	I/O
SA_DQ[29]	AW7	DDR3	I/O
SA_DQ[30]	AW9	DDR3	I/O
SA_DQ[31]	AY9	DDR3	I/O
SA_DQ[32]	AU35	DDR3	I/O
SA_DQ[33]	AW37	DDR3	I/O
SA_DQ[34]	AU39	DDR3	I/O
SA_DQ[35]	AU36	DDR3	I/O
SA_DQ[36]	AW35	DDR3	I/O
SA_DQ[37]	AY36	DDR3	I/O
SA_DQ[38]	AU38	DDR3	I/O
SA_DQ[39]	AU37	DDR3	I/O
SA_DQ[40]	AR40	DDR3	I/O
SA_DQ[41]	AR37	DDR3	I/O
SA_DQ[42]	AN38	DDR3	I/O
SA_DQ[43]	AN37	DDR3	I/O
SA_DQ[44]	AR39	DDR3	I/O
SA_DQ[45]	AR38	DDR3	I/O
SA_DQ[46]	AN39	DDR3	I/O
SA_DQ[47]	AN40	DDR3	I/O
SA_DQ[48]	AL40	DDR3	I/O
SA_DQ[49]	AL37	DDR3	I/O
SA_DQ[50]	AJ38	DDR3	I/O
SA_DQ[51]	AJ37	DDR3	I/O
SA_DQ[52]	AL39	DDR3	I/O
SA_DQ[53]	AL38	DDR3	I/O
SA_DQ[54]	AJ39	DDR3	I/O
SA_DQ[55]	AJ40	DDR3	I/O
SA_DQ[56]	AG40	DDR3	I/O
SA_DQ[57]	AG37	DDR3	I/O
SA_DQ[58]	AE38	DDR3	I/O
SA_DQ[59]	AE37	DDR3	I/O
SA_DQ[60]	AG39	DDR3	I/O
SA_DQ[61]	AG38	DDR3	I/O
SA_DQ[62]	AE39	DDR3	I/O
SA_DQ[63]	AE40	DDR3	I/O
SA_DQS[0]	AK3	DDR3	I/O
SA_DQS[1]	AP3	DDR3	I/O
SA_DQS[2]	AW4	DDR3	I/O
SA_DQS[3]	AV8	DDR3	I/O
SA_DQS[4]	AV37	DDR3	I/O
SA_DQS[5]	AP38	DDR3	I/O
SA_DQS[6]	AK38	DDR3	I/O
SA_DQS[7]	AF38	DDR3	I/O
SA_DQS[8]	AV13	DDR3	I/O
SA_DQS#[0]	AK2	DDR3	I/O
SA_DQS#[1]	AP2	DDR3	I/O
SA_DQS#[2]	AV4	DDR3	I/O
SA_DQS#[3]	AW8	DDR3	I/O
SA_DQS#[4]	AV36	DDR3	I/O
SA_DQS#[5]	AP39	DDR3	I/O
SA_DQS#[6]	AK39	DDR3	I/O
SA_DQS#[7]	AF39	DDR3	I/O
SA_DQS#[8]	AV12	DDR3	I/O
RSVD	AU12	DDR3	I/O
RSVD	AU14	DDR3	I/O
RSVD	AW13	DDR3	I/O
RSVD	AY13	DDR3	I/O
RSVD	AU13	DDR3	I/O
RSVD	AU11	DDR3	I/O
RSVD	AY12	DDR3	I/O
RSVD	AW12	DDR3	I/O
SA_MA[0]	AV27	DDR3	O
SA_MA[1]	AY24	DDR3	O
SA_MA[2]	AW24	DDR3	O
SA_MA[3]	AW23	DDR3	O
SA_MA[4]	AV23	DDR3	O
SA_MA[5]	AT24	DDR3	O
SA_MA[6]	AT23	DDR3	O
SA_MA[7]	AU22	DDR3	O
SA_MA[8]	AV22	DDR3	O
SA_MA[9]	AT22	DDR3	O
SA_MA[10]	AV28	DDR3	O
SA_MA[11]	AU21	DDR3	O
SA_MA[12]	AT21	DDR3	O
SA_MA[13]	AW32	DDR3	O
SA_MA[14]	AU20	DDR3	O
SA_MA[15]	AT20	DDR3	O
SA_ODT[0]	AV31	DDR3	O
SA_ODT[1]	AU32	DDR3	O
SA_ODT[2]	AU30	DDR3	O
SA_ODT[3]	AW33	DDR3	O
SA_RAS#	AU28	DDR3	O
SA_WE#	AW29	DDR3	O
SB_BS[0]	AP23	DDR3	O
SB_BS[1]	AM24	DDR3	O

Table 8-1. Processor Pin List by Pin Name

Pin Name	Pin #	Buffer Type	Dir.
SB_BS[2]	AW17	DDR3	O
SB_CAS#	AK25	DDR3	O
SB_CK[0]	AL21	DDR3	O
SB_CK[1]	AL20	DDR3	O
SB_CK[2]	AL23	DDR3	O
SB_CK[3]	AP21	DDR3	O
SB_CK#[0]	AL22	DDR3	O
SB_CK#[1]	AK20	DDR3	O
SB_CK#[2]	AM22	DDR3	O
SB_CK#[3]	AN21	DDR3	O
SB_CKE[0]	AU16	DDR3	O
SB_CKE[1]	AY15	DDR3	O
SB_CKE[2]	AW15	DDR3	O
SB_CKE[3]	AV15	DDR3	O
SB_CS#[0]	AN25	DDR3	O
SB_CS#[1]	AN26	DDR3	O
SB_CS#[2]	AL25	DDR3	O
SB_CS#[3]	AT26	DDR3	O
SB_DQ[0]	AG7	DDR3	I/O
SB_DQ[1]	AG8	DDR3	I/O
SB_DQ[2]	AJ9	DDR3	I/O
SB_DQ[3]	AJ8	DDR3	I/O
SB_DQ[4]	AG5	DDR3	I/O
SB_DQ[5]	AG6	DDR3	I/O
SB_DQ[6]	AJ6	DDR3	I/O
SB_DQ[7]	AJ7	DDR3	I/O
SB_DQ[8]	AL7	DDR3	I/O
SB_DQ[9]	AM7	DDR3	I/O
SB_DQ[10]	AM10	DDR3	I/O
SB_DQ[11]	AL10	DDR3	I/O
SB_DQ[12]	AL6	DDR3	I/O
SB_DQ[13]	AM6	DDR3	I/O
SB_DQ[14]	AL9	DDR3	I/O
SB_DQ[15]	AM9	DDR3	I/O
SB_DQ[16]	AP7	DDR3	I/O
SB_DQ[17]	AR7	DDR3	I/O
SB_DQ[18]	AP10	DDR3	I/O
SB_DQ[19]	AR10	DDR3	I/O
SB_DQ[20]	AP6	DDR3	I/O
SB_DQ[21]	AR6	DDR3	I/O
SB_DQ[22]	AP9	DDR3	I/O
SB_DQ[23]	AR9	DDR3	I/O
SB_DQ[24]	AM12	DDR3	I/O
SB_DQ[25]	AM13	DDR3	I/O

Table 8-1. Processor Pin List by Pin Name

Pin Name	Pin #	Buffer Type	Dir.
SB_DQ[26]	AR13	DDR3	I/O
SB_DQ[27]	AP13	DDR3	I/O
SB_DQ[28]	AL12	DDR3	I/O
SB_DQ[29]	AL13	DDR3	I/O
SB_DQ[30]	AR12	DDR3	I/O
SB_DQ[31]	AP12	DDR3	I/O
SB_DQ[32]	AR28	DDR3	I/O
SB_DQ[33]	AR29	DDR3	I/O
SB_DQ[34]	AL28	DDR3	I/O
SB_DQ[35]	AL29	DDR3	I/O
SB_DQ[36]	AP28	DDR3	I/O
SB_DQ[37]	AP29	DDR3	I/O
SB_DQ[38]	AM28	DDR3	I/O
SB_DQ[39]	AM29	DDR3	I/O
SB_DQ[40]	AP32	DDR3	I/O
SB_DQ[41]	AP31	DDR3	I/O
SB_DQ[42]	AP35	DDR3	I/O
SB_DQ[43]	AP34	DDR3	I/O
SB_DQ[44]	AR32	DDR3	I/O
SB_DQ[45]	AR31	DDR3	I/O
SB_DQ[46]	AR35	DDR3	I/O
SB_DQ[47]	AR34	DDR3	I/O
SB_DQ[48]	AM32	DDR3	I/O
SB_DQ[49]	AM31	DDR3	I/O
SB_DQ[50]	AL35	DDR3	I/O
SB_DQ[51]	AL32	DDR3	I/O
SB_DQ[52]	AM34	DDR3	I/O
SB_DQ[53]	AL31	DDR3	I/O
SB_DQ[54]	AM35	DDR3	I/O
SB_DQ[55]	AL34	DDR3	I/O
SB_DQ[56]	AH35	DDR3	I/O
SB_DQ[57]	AH34	DDR3	I/O
SB_DQ[58]	AE34	DDR3	I/O
SB_DQ[59]	AE35	DDR3	I/O
SB_DQ[60]	AJ35	DDR3	I/O
SB_DQ[61]	AJ34	DDR3	I/O
SB_DQ[62]	AF33	DDR3	I/O
SB_DQ[63]	AF35	DDR3	I/O
SB_DQS[0]	AH7	DDR3	I/O
SB_DQS[1]	AM8	DDR3	I/O
SB_DQS[2]	AR8	DDR3	I/O
SB_DQS[3]	AN13	DDR3	I/O
SB_DQS[4]	AN29	DDR3	I/O
SB_DQS[5]	AP33	DDR3	I/O

Table 8-1. Processor Pin List by Pin Name

Pin Name	Pin #	Buffer Type	Dir.
SB_DQS[6]	AL33	DDR3	I/O
SB_DQS[7]	AG35	DDR3	I/O
SB_DQS[8]	AN16	DDR3	I/O
SB_DQS#[0]	AH6	DDR3	I/O
SB_DQS#[1]	AL8	DDR3	I/O
SB_DQS#[2]	AP8	DDR3	I/O
SB_DQS#[3]	AN12	DDR3	I/O
SB_DQS#[4]	AN28	DDR3	I/O
SB_DQS#[5]	AR33	DDR3	I/O
SB_DQS#[6]	AM33	DDR3	I/O
SB_DQS#[7]	AG34	DDR3	I/O
SB_DQS#[8]	AN15	DDR3	I/O
RSVD	AL16	DDR3	I/O
RSVD	AM16	DDR3	I/O
RSVD	AP16	DDR3	I/O
RSVD	AR16	DDR3	I/O
RSVD	AL15	DDR3	I/O
RSVD	AM15	DDR3	I/O
RSVD	AR15	DDR3	I/O
RSVD	AP15	DDR3	I/O
SB_MA[0]	AK24	DDR3	O
SB_MA[1]	AM20	DDR3	O
SB_MA[2]	AM19	DDR3	O
SB_MA[3]	AK18	DDR3	O
SB_MA[4]	AP19	DDR3	O
SB_MA[5]	AP18	DDR3	O
SB_MA[6]	AM18	DDR3	O
SB_MA[7]	AL18	DDR3	O
SB_MA[8]	AN18	DDR3	O
SB_MA[9]	AY17	DDR3	O
SB_MA[10]	AN23	DDR3	O
SB_MA[11]	AU17	DDR3	O
SB_MA[12]	AT18	DDR3	O
SB_MA[13]	AR26	DDR3	O
SB_MA[14]	AY16	DDR3	O
SB_MA[15]	AV16	DDR3	O
SB_ODT[0]	AL26	DDR3	O
SB_ODT[1]	AP26	DDR3	O
SB_ODT[2]	AM26	DDR3	O
SB_ODT[3]	AK26	DDR3	O
SB_RAS#	AP24	DDR3	O
SB_WE#	AR25	DDR3	O
SKTOCC#	AJ33	Analog	O
SM_DRAMPWROK	AJ19	Async CMOS	I

Table 8-1. Processor Pin List by Pin Name

Pin Name	Pin #	Buffer Type	Dir.
SM_DRAMRST#	AW18	DDR3	O
SM_VREF	AJ22	Analog	I
TCK	M40	TAP	I
TDI	L40	TAP	I
TDO	L39	TAP	O
THERMTRIP#	G35	Async CMOS	O
TMS	L38	TAP	I
TRST#	J39	TAP	I
UNCOREPWRGOOD	J40	Async CMOS	I
VCC	A12	PWR	
VCC	A13	PWR	
VCC	A14	PWR	
VCC	A15	PWR	
VCC	A16	PWR	
VCC	A18	PWR	
VCC	A24	PWR	
VCC	A25	PWR	
VCC	A27	PWR	
VCC	A28	PWR	
VCC	B15	PWR	
VCC	B16	PWR	
VCC	B18	PWR	
VCC	B24	PWR	
VCC	B25	PWR	
VCC	B27	PWR	
VCC	B28	PWR	
VCC	B30	PWR	
VCC	B31	PWR	
VCC	B33	PWR	
VCC	B34	PWR	
VCC	C15	PWR	
VCC	C16	PWR	
VCC	C18	PWR	
VCC	C19	PWR	
VCC	C21	PWR	
VCC	C22	PWR	
VCC	C24	PWR	
VCC	C25	PWR	
VCC	C27	PWR	
VCC	C28	PWR	
VCC	C30	PWR	
VCC	C31	PWR	
VCC	C33	PWR	
VCC	C34	PWR	

Table 8-1. Processor Pin List by Pin Name

Pin Name	Pin #	Buffer Type	Dir.
VCC	C36	PWR	
VCC	D13	PWR	
VCC	D14	PWR	
VCC	D15	PWR	
VCC	D16	PWR	
VCC	D18	PWR	
VCC	D19	PWR	
VCC	D21	PWR	
VCC	D22	PWR	
VCC	D24	PWR	
VCC	D25	PWR	
VCC	D27	PWR	
VCC	D28	PWR	
VCC	D30	PWR	
VCC	D31	PWR	
VCC	D33	PWR	
VCC	D34	PWR	
VCC	D35	PWR	
VCC	D36	PWR	
VCC	E15	PWR	
VCC	E16	PWR	
VCC	E18	PWR	
VCC	E19	PWR	
VCC	E21	PWR	
VCC	E22	PWR	
VCC	E24	PWR	
VCC	E25	PWR	
VCC	E27	PWR	
VCC	E28	PWR	
VCC	E30	PWR	
VCC	E31	PWR	
VCC	E33	PWR	
VCC	E34	PWR	
VCC	E35	PWR	
VCC	F15	PWR	
VCC	F16	PWR	
VCC	F18	PWR	
VCC	F19	PWR	
VCC	F21	PWR	
VCC	F22	PWR	
VCC	F24	PWR	
VCC	F25	PWR	
VCC	F27	PWR	
VCC	F28	PWR	
VCC	F30	PWR	
VCC	F31	PWR	
VCC	F32	PWR	
VCC	F33	PWR	
VCC	F34	PWR	
VCC	G15	PWR	
VCC	G16	PWR	
VCC	G18	PWR	
VCC	G19	PWR	
VCC	G21	PWR	
VCC	G22	PWR	
VCC	G24	PWR	
VCC	G25	PWR	
VCC	G27	PWR	
VCC	G28	PWR	
VCC	G30	PWR	
VCC	G31	PWR	
VCC	G32	PWR	
VCC	G33	PWR	
VCC	H13	PWR	
VCC	H14	PWR	
VCC	H15	PWR	
VCC	H16	PWR	
VCC	H18	PWR	
VCC	H19	PWR	
VCC	H21	PWR	
VCC	H22	PWR	
VCC	H24	PWR	
VCC	H25	PWR	
VCC	H27	PWR	
VCC	H28	PWR	
VCC	H30	PWR	
VCC	H31	PWR	
VCC	H32	PWR	
VCC	J12	PWR	
VCC	J15	PWR	
VCC	J16	PWR	
VCC	J18	PWR	
VCC	J19	PWR	
VCC	J21	PWR	
VCC	J22	PWR	
VCC	J24	PWR	
VCC	J25	PWR	
VCC	J27	PWR	

Table 8-1. Processor Pin List by Pin Name

Pin Name	Pin #	Buffer Type	Dir.
VCC	J28	PWR	
VCC	J30	PWR	
VCC	K15	PWR	
VCC	K16	PWR	
VCC	K18	PWR	
VCC	K19	PWR	
VCC	K21	PWR	
VCC	K22	PWR	
VCC	K24	PWR	
VCC	K25	PWR	
VCC	K27	PWR	
VCC	K28	PWR	
VCC	K30	PWR	
VCC	L13	PWR	
VCC	L14	PWR	
VCC	L15	PWR	
VCC	L16	PWR	
VCC	L18	PWR	
VCC	L19	PWR	
VCC	L21	PWR	
VCC	L22	PWR	
VCC	L24	PWR	
VCC	L25	PWR	
VCC	L27	PWR	
VCC	L28	PWR	
VCC	L30	PWR	
VCC	M14	PWR	
VCC	M15	PWR	
VCC	M16	PWR	
VCC	M18	PWR	
VCC	M19	PWR	
VCC	M21	PWR	
VCC	M22	PWR	
VCC	M24	PWR	
VCC	M25	PWR	
VCC	M27	PWR	
VCC	M28	PWR	
VCC	M30	PWR	
VCC_SENSE	A36	Analog	O
VCCAXG	AB33	PWR	
VCCAXG	AB34	PWR	
VCCAXG	AB35	PWR	
VCCAXG	AB36	PWR	
VCCAXG	AB37	PWR	

Table 8-1. Processor Pin List by Pin Name

Pin Name	Pin #	Buffer Type	Dir.
VCCAXG	AB38	PWR	
VCCAXG	AB39	PWR	
VCCAXG	AB40	PWR	
VCCAXG	AC33	PWR	
VCCAXG	AC34	PWR	
VCCAXG	AC35	PWR	
VCCAXG	AC36	PWR	
VCCAXG	AC37	PWR	
VCCAXG	AC38	PWR	
VCCAXG	AC39	PWR	
VCCAXG	AC40	PWR	
VCCAXG	T33	PWR	
VCCAXG	T34	PWR	
VCCAXG	T35	PWR	
VCCAXG	T36	PWR	
VCCAXG	T37	PWR	
VCCAXG	T38	PWR	
VCCAXG	T39	PWR	
VCCAXG	T40	PWR	
VCCAXG	U33	PWR	
VCCAXG	U34	PWR	
VCCAXG	U35	PWR	
VCCAXG	U36	PWR	
VCCAXG	U37	PWR	
VCCAXG	U38	PWR	
VCCAXG	U39	PWR	
VCCAXG	U40	PWR	
VCCAXG	W33	PWR	
VCCAXG	W34	PWR	
VCCAXG	W35	PWR	
VCCAXG	W36	PWR	
VCCAXG	W37	PWR	
VCCAXG	W38	PWR	
VCCAXG	Y33	PWR	
VCCAXG	Y34	PWR	
VCCAXG	Y35	PWR	
VCCAXG	Y36	PWR	
VCCAXG	Y37	PWR	
VCCAXG	Y38	PWR	
VCCAXG_SENSE	L32	Analog	O
VCCIO	A11	PWR	
VCCIO	A7	PWR	
VCCIO	AA3	PWR	
VCCIO	AB8	PWR	

Table 8-1. Processor Pin List by Pin Name

Pin Name	Pin #	Buffer Type	Dir.
VCCIO	AF8	PWR	
VCCIO	AG33	PWR	
VCCIO	AJ16	PWR	
VCCIO	AJ17	PWR	
VCCIO	AJ26	PWR	
VCCIO	AJ28	PWR	
VCCIO	AJ32	PWR	
VCCIO	AK15	PWR	
VCCIO	AK17	PWR	
VCCIO	AK19	PWR	
VCCIO	AK21	PWR	
VCCIO	AK23	PWR	
VCCIO	AK27	PWR	
VCCIO	AK29	PWR	
VCCIO	AK30	PWR	
VCCIO	B9	PWR	
VCCIO	D10	PWR	
VCCIO	D6	PWR	
VCCIO	E3	PWR	
VCCIO	E4	PWR	
VCCIO	G3	PWR	
VCCIO	G4	PWR	
VCCIO	J3	PWR	
VCCIO	J4	PWR	
VCCIO	J7	PWR	
VCCIO	J8	PWR	
VCCIO	L3	PWR	
VCCIO	L4	PWR	
VCCIO	L7	PWR	
VCCIO	M13	PWR	
VCCIO	N3	PWR	
VCCIO	N4	PWR	
VCCIO	N7	PWR	
VCCIO	R3	PWR	
VCCIO	R4	PWR	
VCCIO	R7	PWR	
VCCIO	U3	PWR	
VCCIO	U4	PWR	
VCCIO	U7	PWR	
VCCIO	V8	PWR	
VCCIO	W3	PWR	
VCCIO_SEL	P33	N/A	O
VCCIO_SENSE	AB4	Analog	O
VCCPLL	AK11	PWR	
VCCPLL	AK12	PWR	
VCCSA	H10	PWR	
VCCSA	H11	PWR	
VCCSA	H12	PWR	
VCCSA	J10	PWR	
VCCSA	K10	PWR	
VCCSA	K11	PWR	
VCCSA	L11	PWR	
VCCSA	L12	PWR	
VCCSA	M10	PWR	
VCCSA	M11	PWR	
VCCSA	M12	PWR	
VCCSA_SENSE	T2	Analog	O
VCCSA_VID	P34	CMOS	O
VDDQ	AJ13	PWR	
VDDQ	AJ14	PWR	
VDDQ	AJ20	PWR	
VDDQ	AJ23	PWR	
VDDQ	AJ24	PWR	
VDDQ	AR20	PWR	
VDDQ	AR21	PWR	
VDDQ	AR22	PWR	
VDDQ	AR23	PWR	
VDDQ	AR24	PWR	
VDDQ	AU19	PWR	
VDDQ	AU23	PWR	
VDDQ	AU27	PWR	
VDDQ	AU31	PWR	
VDDQ	AV21	PWR	
VDDQ	AV24	PWR	
VDDQ	AV25	PWR	
VDDQ	AV29	PWR	
VDDQ	AV33	PWR	
VDDQ	AW31	PWR	
VDDQ	AY23	PWR	
VDDQ	AY26	PWR	
VDDQ	AY28	PWR	
VIDALERT#	A37	CMOS	I
VIDSCLK	C37	CMOS	O
VIDSOUT	B37	CMOS	I/O
VSS	A17	GND	
VSS	A23	GND	
VSS	A26	GND	
VSS	A29	GND	

Table 8-1. Processor Pin List by Pin Name

Pin Name	Pin #	Buffer Type	Dir.
VSS	A35	GND	
VSS	AA33	GND	
VSS	AA34	GND	
VSS	AA35	GND	
VSS	AA36	GND	
VSS	AA37	GND	
VSS	AA38	GND	
VSS	AA6	GND	
VSS	AB5	GND	
VSS	AC1	GND	
VSS	AC6	GND	
VSS	AD33	GND	
VSS	AD36	GND	
VSS	AD38	GND	
VSS	AD39	GND	
VSS	AD40	GND	
VSS	AD5	GND	
VSS	AD8	GND	
VSS	AE3	GND	
VSS	AE33	GND	
VSS	AE36	GND	
VSS	AF1	GND	
VSS	AF34	GND	
VSS	AF36	GND	
VSS	AF37	GND	
VSS	AF40	GND	
VSS	AF5	GND	
VSS	AF6	GND	
VSS	AF7	GND	
VSS	AG36	GND	
VSS	AH2	GND	
VSS	AH3	GND	
VSS	AH33	GND	
VSS	AH36	GND	
VSS	AH37	GND	
VSS	AH38	GND	
VSS	AH39	GND	
VSS	AH40	GND	
VSS	AH5	GND	
VSS	AH8	GND	
VSS	AJ12	GND	
VSS	AJ15	GND	
VSS	AJ18	GND	
VSS	AJ21	GND	
VSS	AJ25	GND	
VSS	AJ27	GND	
VSS	AJ36	GND	
VSS	AJ5	GND	
VSS	AK1	GND	
VSS	AK10	GND	
VSS	AK13	GND	
VSS	AK14	GND	
VSS	AK16	GND	
VSS	AK22	GND	
VSS	AK28	GND	
VSS	AK31	GND	
VSS	AK32	GND	
VSS	AK33	GND	
VSS	AK34	GND	
VSS	AK35	GND	
VSS	AK36	GND	
VSS	AK37	GND	
VSS	AK4	GND	
VSS	AK40	GND	
VSS	AK5	GND	
VSS	AK6	GND	
VSS	AK7	GND	
VSS	AK8	GND	
VSS	AK9	GND	
VSS	AL11	GND	
VSS	AL14	GND	
VSS	AL17	GND	
VSS	AL19	GND	
VSS	AL24	GND	
VSS	AL27	GND	
VSS	AL30	GND	
VSS	AL36	GND	
VSS	AL5	GND	
VSS	AM1	GND	
VSS	AM11	GND	
VSS	AM14	GND	
VSS	AM17	GND	
VSS	AM2	GND	
VSS	AM21	GND	
VSS	AM23	GND	
VSS	AM25	GND	
VSS	AM27	GND	
VSS	AM3	GND	

Table 8-1. Processor Pin List by Pin Name

Pin Name	Pin #	Buffer Type	Dir.
VSS	AM30	GND	
VSS	AM36	GND	
VSS	AM37	GND	
VSS	AM38	GND	
VSS	AM39	GND	
VSS	AM4	GND	
VSS	AM40	GND	
VSS	AM5	GND	
VSS	AN10	GND	
VSS	AN11	GND	
VSS	AN14	GND	
VSS	AN17	GND	
VSS	AN19	GND	
VSS	AN22	GND	
VSS	AN24	GND	
VSS	AN27	GND	
VSS	AN30	GND	
VSS	AN31	GND	
VSS	AN32	GND	
VSS	AN33	GND	
VSS	AN34	GND	
VSS	AN35	GND	
VSS	AN36	GND	
VSS	AN5	GND	
VSS	AN6	GND	
VSS	AN7	GND	
VSS	AN8	GND	
VSS	AN9	GND	
VSS	AP1	GND	
VSS	AP11	GND	
VSS	AP14	GND	
VSS	AP17	GND	
VSS	AP22	GND	
VSS	AP25	GND	
VSS	AP27	GND	
VSS	AP30	GND	
VSS	AP36	GND	
VSS	AP37	GND	
VSS	AP4	GND	
VSS	AP40	GND	
VSS	AP5	GND	
VSS	AR11	GND	
VSS	AR14	GND	
VSS	AR17	GND	

Table 8-1. Processor Pin List by Pin Name

Pin Name	Pin #	Buffer Type	Dir.
VSS	AR18	GND	
VSS	AR19	GND	
VSS	AR27	GND	
VSS	AR30	GND	
VSS	AR36	GND	
VSS	AR5	GND	
VSS	AT1	GND	
VSS	AT10	GND	
VSS	AT12	GND	
VSS	AT13	GND	
VSS	AT15	GND	
VSS	AT16	GND	
VSS	AT17	GND	
VSS	AT2	GND	
VSS	AT25	GND	
VSS	AT27	GND	
VSS	AT28	GND	
VSS	AT29	GND	
VSS	AT3	GND	
VSS	AT30	GND	
VSS	AT31	GND	
VSS	AT32	GND	
VSS	AT33	GND	
VSS	AT34	GND	
VSS	AT35	GND	
VSS	AT36	GND	
VSS	AT37	GND	
VSS	AT38	GND	
VSS	AT39	GND	
VSS	AT4	GND	
VSS	AT40	GND	
VSS	AT5	GND	
VSS	AT6	GND	
VSS	AT7	GND	
VSS	AT8	GND	
VSS	AT9	GND	
VSS	AU1	GND	
VSS	AU15	GND	
VSS	AU26	GND	
VSS	AU34	GND	
VSS	AU4	GND	
VSS	AU6	GND	
VSS	AU8	GND	
VSS	AV10	GND	

Table 8-1. Processor Pin List by Pin Name

Pin Name	Pin #	Buffer Type	Dir.
VSS	AV11	GND	
VSS	AV14	GND	
VSS	AV17	GND	
VSS	AV3	GND	
VSS	AV35	GND	
VSS	AV38	GND	
VSS	AV6	GND	
VSS	AW10	GND	
VSS	AW11	GND	
VSS	AW14	GND	
VSS	AW16	GND	
VSS	AW36	GND	
VSS	AW6	GND	
VSS	AY11	GND	
VSS	AY14	GND	
VSS	AY18	GND	
VSS	AY35	GND	
VSS	AY4	GND	
VSS	AY6	GND	
VSS	AY8	GND	
VSS	B10	GND	
VSS	B13	GND	
VSS	B14	GND	
VSS	B17	GND	
VSS	B23	GND	
VSS	B26	GND	
VSS	B29	GND	
VSS	B32	GND	
VSS	B35	GND	
VSS	B38	GND	
VSS	B6	GND	
VSS	C11	GND	
VSS	C12	GND	
VSS	C17	GND	
VSS	C20	GND	
VSS	C23	GND	
VSS	C26	GND	
VSS	C29	GND	
VSS	C32	GND	
VSS	C35	GND	
VSS	C7	GND	
VSS	C8	GND	
VSS	D17	GND	
VSS	D2	GND	

Table 8-1. Processor Pin List by Pin Name

Pin Name	Pin #	Buffer Type	Dir.
VSS	D20	GND	
VSS	D23	GND	
VSS	D26	GND	
VSS	D29	GND	
VSS	D32	GND	
VSS	D37	GND	
VSS	D39	GND	
VSS	D4	GND	
VSS	D5	GND	
VSS	D9	GND	
VSS	E11	GND	
VSS	E12	GND	
VSS	E17	GND	
VSS	E20	GND	
VSS	E23	GND	
VSS	E26	GND	
VSS	E29	GND	
VSS	E32	GND	
VSS	E36	GND	
VSS	E7	GND	
VSS	E8	GND	
VSS	F1	GND	
VSS	F10	GND	
VSS	F13	GND	
VSS	F14	GND	
VSS	F17	GND	
VSS	F2	GND	
VSS	F20	GND	
VSS	F23	GND	
VSS	F26	GND	
VSS	F29	GND	
VSS	F35	GND	
VSS	F37	GND	
VSS	F39	GND	
VSS	F5	GND	
VSS	F6	GND	
VSS	F9	GND	
VSS	G11	GND	
VSS	G12	GND	
VSS	G17	GND	
VSS	G20	GND	
VSS	G23	GND	
VSS	G26	GND	
VSS	G29	GND	

Table 8-1. Processor Pin List by Pin Name

Pin Name	Pin #	Buffer Type	Dir.
VSS	G34	GND	
VSS	G7	GND	
VSS	G8	GND	
VSS	H1	GND	
VSS	H17	GND	
VSS	H2	GND	
VSS	H20	GND	
VSS	H23	GND	
VSS	H26	GND	
VSS	H29	GND	
VSS	H33	GND	
VSS	H35	GND	
VSS	H37	GND	
VSS	H39	GND	
VSS	H5	GND	
VSS	H6	GND	
VSS	H9	GND	
VSS	J11	GND	
VSS	J17	GND	
VSS	J20	GND	
VSS	J23	GND	
VSS	J26	GND	
VSS	J29	GND	
VSS	J32	GND	
VSS	K1	GND	
VSS	K12	GND	
VSS	K13	GND	
VSS	K14	GND	
VSS	K17	GND	
VSS	K2	GND	
VSS	K20	GND	
VSS	K23	GND	
VSS	K26	GND	
VSS	K29	GND	
VSS	K33	GND	
VSS	K35	GND	
VSS	K37	GND	
VSS	K39	GND	
VSS	K5	GND	
VSS	K6	GND	
VSS	L10	GND	
VSS	L17	GND	
VSS	L20	GND	
VSS	L23	GND	
VSS	L26	GND	
VSS	L29	GND	
VSS	L8	GND	
VSS	M1	GND	
VSS	M17	GND	
VSS	M2	GND	
VSS	M20	GND	
VSS	M23	GND	
VSS	M26	GND	
VSS	M29	GND	
VSS	M33	GND	
VSS	M35	GND	
VSS	M37	GND	
VSS	M39	GND	
VSS	M5	GND	
VSS	M6	GND	
VSS	M9	GND	
VSS	N8	GND	
VSS	P1	GND	
VSS	P2	GND	
VSS	P36	GND	
VSS	P38	GND	
VSS	P40	GND	
VSS	P5	GND	
VSS	P6	GND	
VSS	R33	GND	
VSS	R35	GND	
VSS	R37	GND	
VSS	R39	GND	
VSS	R8	GND	
VSS	T1	GND	
VSS	T5	GND	
VSS	T6	GND	
VSS	U8	GND	
VSS	V1	GND	
VSS	V2	GND	
VSS	V33	GND	
VSS	V34	GND	
VSS	V35	GND	
VSS	V36	GND	
VSS	V37	GND	
VSS	V38	GND	
VSS	V39	GND	
VSS	V40	GND	

Table 8-1. Processor Pin List by Pin Name

Pin Name	Pin #	Buffer Type	Dir.
VSS	V5	GND	
VSS	W6	GND	
VSS	Y5	GND	
VSS	Y8	GND	
VSS_NCTF	A4	GND	
VSS_NCTF	AV39	GND	
VSS_NCTF	AY37	GND	
VSS_NCTF	B3	GND	
VSS_SENSE	B36	Analog	O
VSSAXG_SENSE	M32	Analog	O
VSSIO_SENSE	AB3	Analog	O

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9 DDR Data Swizzling

To achieve better memory performance and better memory timing, Intel design performed the DDR Data pin swizzling that will allow a better use of the product across different platforms. Swizzling has no effect on functional operation and is invisible to the OS/SW.

However, during debug, swizzling needs to be taken into consideration. This chapter presents swizzling data. When placing a DIMM logic analyzer, the design engineer must pay attention to the swizzling table to perform an efficient memory debug.

Table 9-1. DDR Data Swizzling Table – Channel A

Pin Name	Pin #	MC Pin Name
SA_DQ[0]	AJ3	DQ01
SA_DQ[1]	AJ4	DQ02
SA_DQ[2]	AL3	DQ07
SA_DQ[3]	AL4	DQ06
SA_DQ[4]	AJ2	DQ03
SA_DQ[5]	AJ1	DQ00
SA_DQ[6]	AL2	DQ05
SA_DQ[7]	AL1	DQ04
SA_DQ[8]	AN1	DQ08
SA_DQ[9]	AN4	DQ11
SA_DQ[10]	AR3	DQ14
SA_DQ[11]	AR4	DQ15
SA_DQ[12]	AN2	DQ09
SA_DQ[13]	AN3	DQ10
SA_DQ[14]	AR2	DQ13
SA_DQ[15]	AR1	DQ12
SA_DQ[16]	AV2	DQ18
SA_DQ[17]	AW3	DQ19
SA_DQ[18]	AV5	DQ22
SA_DQ[19]	AW5	DQ20
SA_DQ[20]	AU2	DQ16
SA_DQ[21]	AU3	DQ17
SA_DQ[22]	AU5	DQ21
SA_DQ[23]	AY5	DQ23
SA_DQ[24]	AY7	DQ27
SA_DQ[25]	AU7	DQ25
SA_DQ[26]	AV9	DQ28
SA_DQ[27]	AU9	DQ29
SA_DQ[28]	AV7	DQ24
SA_DQ[29]	AW7	DQ26
SA_DQ[30]	AW9	DQ30
SA_DQ[31]	AY9	DQ31
SA_DQ[32]	AU35	DQ35
SA_DQ[33]	AW37	DQ34
SA_DQ[34]	AU39	DQ38
SA_DQ[35]	AU36	DQ39
SA_DQ[36]	AW35	DQ33
SA_DQ[37]	AY36	DQ32
SA_DQ[38]	AU38	DQ36
SA_DQ[39]	AU37	DQ37
SA_DQ[40]	AR40	DQ43
SA_DQ[41]	AR37	DQ42
SA_DQ[42]	AN38	DQ44
SA_DQ[43]	AN37	DQ45
SA_DQ[44]	AR39	DQ41
SA_DQ[45]	AR38	DQ40
SA_DQ[46]	AN39	DQ46
SA_DQ[47]	AN40	DQ47
SA_DQ[48]	AL40	DQ51
SA_DQ[49]	AL37	DQ48
SA_DQ[50]	AJ38	DQ52
SA_DQ[51]	AJ37	DQ53
SA_DQ[52]	AL39	DQ49
SA_DQ[53]	AL38	DQ50
SA_DQ[54]	AJ39	DQ54
SA_DQ[55]	AJ40	DQ55
SA_DQ[56]	AG40	DQ58
SA_DQ[57]	AG37	DQ56
SA_DQ[58]	AE38	DQ60
SA_DQ[59]	AE37	DQ61
SA_DQ[60]	AG39	DQ57
SA_DQ[61]	AG38	DQ59
SA_DQ[62]	AE39	DQ63
SA_DQ[63]	AE40	DQ62

Table 9-2. DDR Data Swizzling Table – Channel B

Pin Name	Pin #	MC Pin Name
SB_DQ[0]	AG7	DQ03
SB_DQ[1]	AG8	DQ02
SB_DQ[2]	AJ9	DQ05
SB_DQ[3]	AJ8	DQ04
SB_DQ[4]	AG5	DQ00
SB_DQ[5]	AG6	DQ01
SB_DQ[6]	AJ6	DQ06
SB_DQ[7]	AJ7	DQ07
SB_DQ[8]	AL7	DQ11
SB_DQ[9]	AM7	DQ10
SB_DQ[10]	AM10	DQ14
SB_DQ[11]	AL10	DQ13
SB_DQ[12]	AL6	DQ08
SB_DQ[13]	AM6	DQ09
SB_DQ[14]	AL9	DQ12
SB_DQ[15]	AM9	DQ15
SB_DQ[16]	AP7	DQ19
SB_DQ[17]	AR7	DQ18
SB_DQ[18]	AP10	DQ21
SB_DQ[19]	AR10	DQ22
SB_DQ[20]	AP6	DQ17
SB_DQ[21]	AR6	DQ16
SB_DQ[22]	AP9	DQ20
SB_DQ[23]	AR9	DQ23
SB_DQ[24]	AM12	DQ25
SB_DQ[25]	AM13	DQ30
SB_DQ[26]	AR13	DQ29
SB_DQ[27]	AP13	DQ28
SB_DQ[28]	AL12	DQ24
SB_DQ[29]	AL13	DQ31
SB_DQ[30]	AR12	DQ27
SB_DQ[31]	AP12	DQ26
SB_DQ[32]	AR28	DQ32
SB_DQ[33]	AR29	DQ34
SB_DQ[34]	AL28	DQ39
SB_DQ[35]	AL29	DQ37
SB_DQ[36]	AP28	DQ33
SB_DQ[37]	AP29	DQ35
SB_DQ[38]	AM28	DQ36
SB_DQ[39]	AM29	DQ38
SB_DQ[40]	AP32	DQ44
SB_DQ[41]	AP31	DQ43
SB_DQ[42]	AP35	DQ45
SB_DQ[43]	AP34	DQ46
SB_DQ[44]	AR32	DQ40
SB_DQ[45]	AR31	DQ42
SB_DQ[46]	AR35	DQ47
SB_DQ[47]	AR34	DQ41
SB_DQ[48]	AM32	DQ51
SB_DQ[49]	AM31	DQ48
SB_DQ[50]	AL35	DQ53
SB_DQ[51]	AL32	DQ50
SB_DQ[52]	AM34	DQ52
SB_DQ[53]	AL31	DQ49
SB_DQ[54]	AM35	DQ54
SB_DQ[55]	AL34	DQ55
SB_DQ[56]	AH35	DQ59
SB_DQ[57]	AH34	DQ58
SB_DQ[58]	AE34	DQ61
SB_DQ[59]	AE35	DQ62
SB_DQ[60]	AJ35	DQ57
SB_DQ[61]	AJ34	DQ56
SB_DQ[62]	AF33	DQ63
SB_DQ[63]	AF35	DQ60

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