

P-channel -30 V, 9 mΩ typ., -62 A STripFET™ H6 Power MOSFET in a PowerFLAT 5x6 package

Datasheet - production data

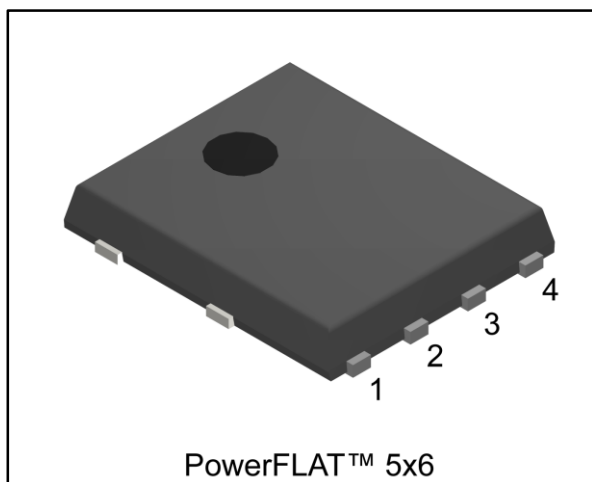
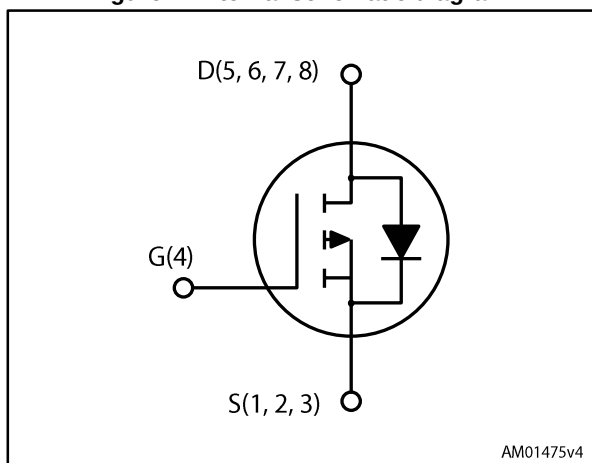


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max	I _D
STL62P3LLH6	-30 V	10.5 mΩ	-62 A

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is a P-channel Power MOSFET developed using the STripFET™ H6 technology, with a new trench gate structure. The resulting Power MOSFET exhibits very low R_{DS(on)} in all packages.

Table 1: Device summary

Order code	Marking	Package	Packing
STL62P3LLH6	62P3LLH6	PowerFLAT™ 5x6	Tape and reel

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
	2.1 Electrical characteristics (curves).....	6
3	Test circuits	9
4	Package information	10
	4.1 PowerFLAT 5x6 type R package information	11
5	Packing information	13
6	Revision history	15

1 Electrical ratings

Table 3: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	-62	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	-44	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^{\circ}\text{C}$	-14	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 100\text{ }^{\circ}\text{C}$	-9.5	A
$I_D^{(1)(2)}$	Drain current (pulsed)	-248	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	-56	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	100	W
$P_{TOT}^{(2)}$	Total dissipation at $T_{pcb} = 25\text{ }^{\circ}\text{C}$	4.8	W
T_{stg}	Storage temperature range	- 55 to 175	$^{\circ}\text{C}$
T_j	Operating junction temperature range		

Notes:

⁽¹⁾The value is rated according to R_{thj-c} .

⁽²⁾This value is rated according to $R_{thj-pcb}$.

⁽³⁾Pulse width is limited by safe operating area.

Table 4: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.5	$^{\circ}\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb, single operation	31.3	$^{\circ}\text{C/W}$

Notes:

⁽¹⁾When mounted on FR-4 board of 1inch², 2oz Cu

2 Electrical characteristics

($T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 5: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = -250\text{ }\mu\text{A}$	-30			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = -30\text{ V}$			-1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = -30\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}^{(1)}$			-10	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = -250\text{ }\mu\text{A}$	-1			V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = -10\text{ V}$, $I_D = -7\text{ A}$		9	10.5	m Ω
		$V_{GS} = -4.5\text{ V}$, $I_D = -7\text{ A}$		13	16	m Ω

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = -25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	3350	-	pF
C_{oss}	Output capacitance		-	414	-	pF
C_{rss}	Reverse transfer capacitance		-	287	-	pF
Q_g	Total gate charge	$V_{DD} = -15\text{ V}$, $I_D = -14\text{ A}$, $V_{GS} = -4.5\text{ V}$ (see Figure 14: "Gate charge test circuit")	-	33	-	nC
Q_{gs}	Gate-source charge		-	14	-	nC
Q_{gd}	Gate-drain charge		-	11	-	nC

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = -15\text{ V}$, $I_D = -7\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = -10\text{ V}$ (see Figure 13: "Switching times test circuit for resistive load")	-	12.8	-	ns
t_r	Rise time		-	112	-	ns
$t_{d(off)}$	Turn-off delay time		-	61	-	ns
t_f	Fall time		-	45	-	ns

Table 8: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = -7\text{ A}$, $V_{GS} = 0\text{ V}$	-		-1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = -24\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = -16\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 15: "Source-drain diode forward characteristics")	-	25.2		ns
Q_{rr}	Reverse recovery charge		-	17.4		nC
I_{RRM}	Reverse recovery current		-	1.4		A

Notes:

⁽¹⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)



Note: For the P-channel Power MOSFET, current and voltage polarities are reversed.

Figure 2: Safe operating area

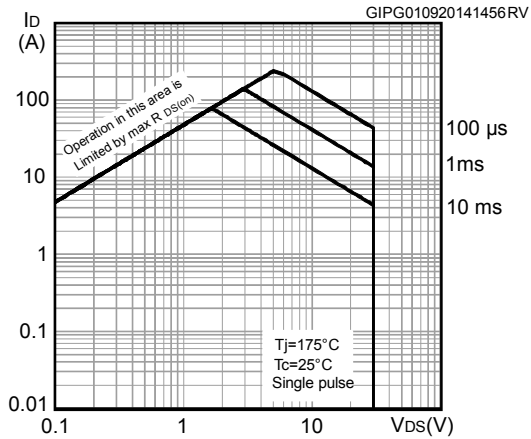


Figure 3: Thermal impedance

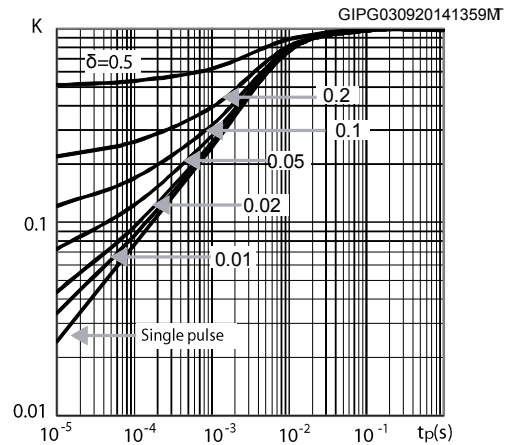


Figure 4: Output characteristics

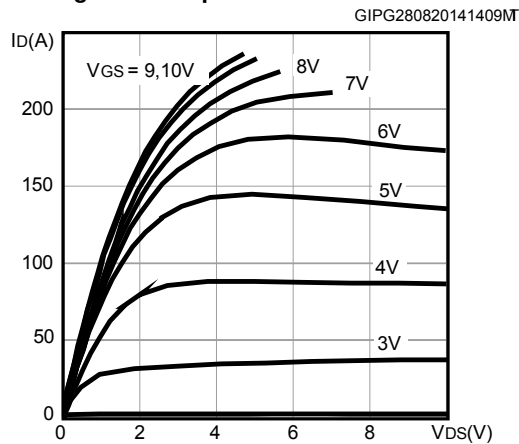


Figure 5: Transfer characteristics

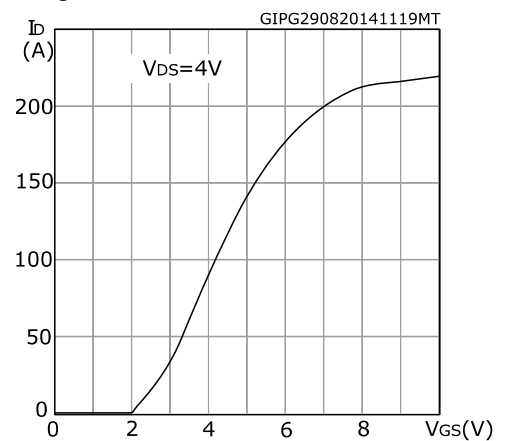


Figure 6: Gate charge vs gate-source voltage

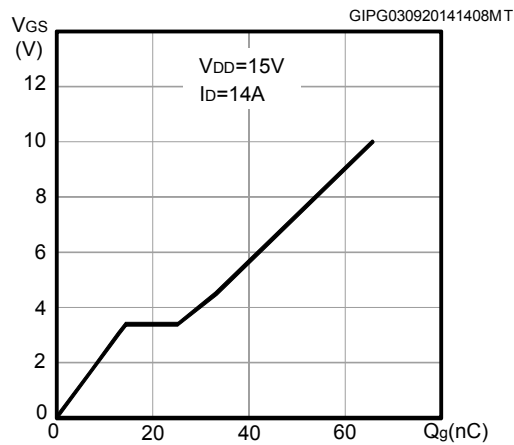


Figure 7: Static drain-source on-resistance

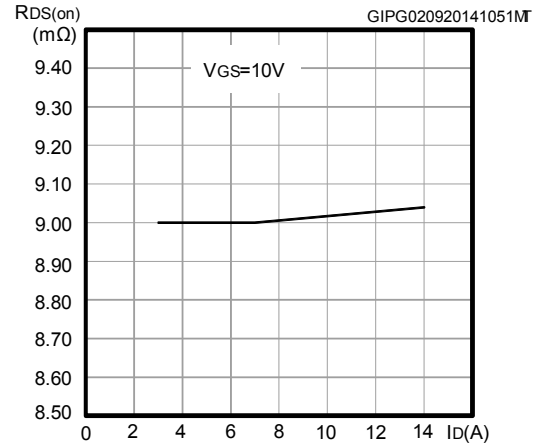


Figure 8: Capacitance variations

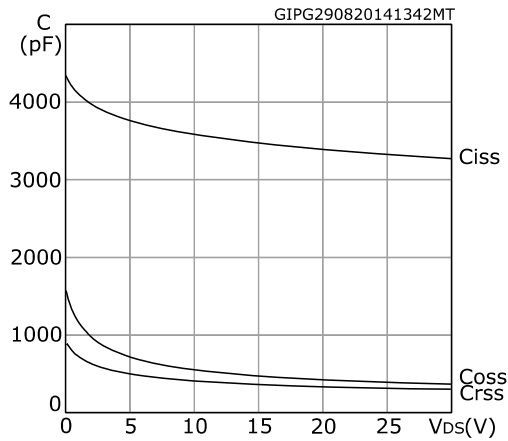


Figure 9: Normalized gate threshold voltage vs temperature

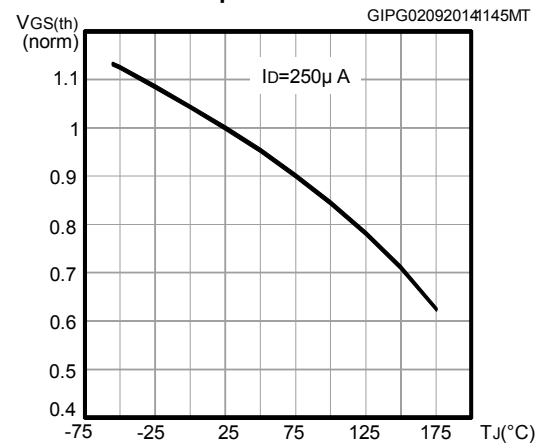


Figure 10: Normalized on-resistance vs temperature

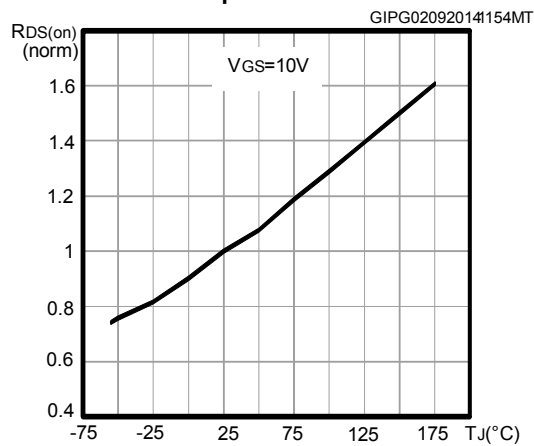


Figure 11: Normalized V(BR)DSS vs temperature

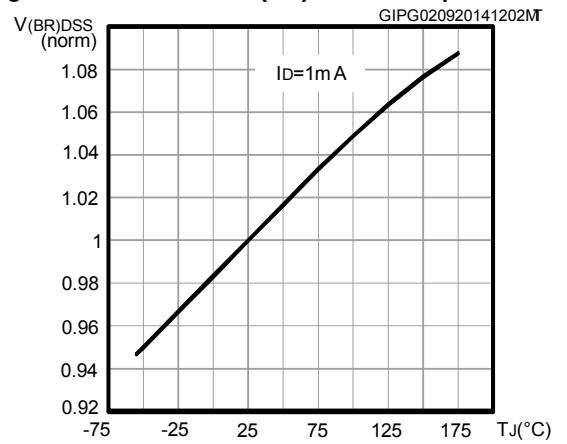
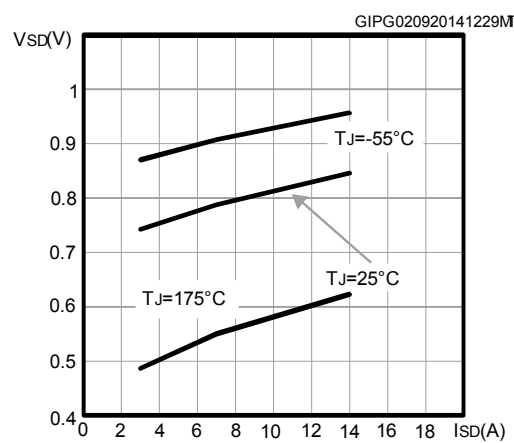


Figure 12: Source-drain diode forward characteristics



3 Test circuits

Figure 13: Switching times test circuit for resistive load

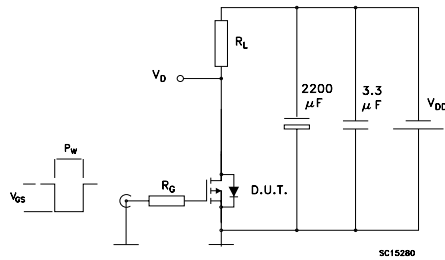


Figure 14: Gate charge test circuit

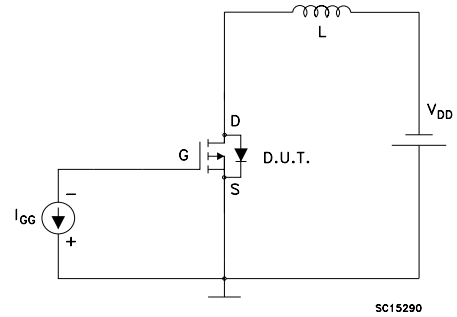
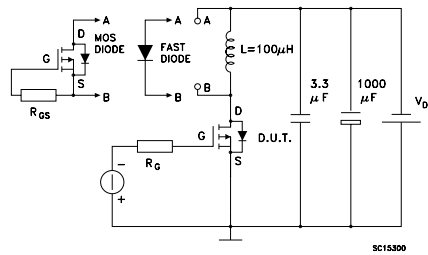


Figure 15: Source-drain diode forward characteristics



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.

4.1 PowerFLAT 5x6 type R package information

Figure 16: PowerFLAT™ 5x6 type R package outline

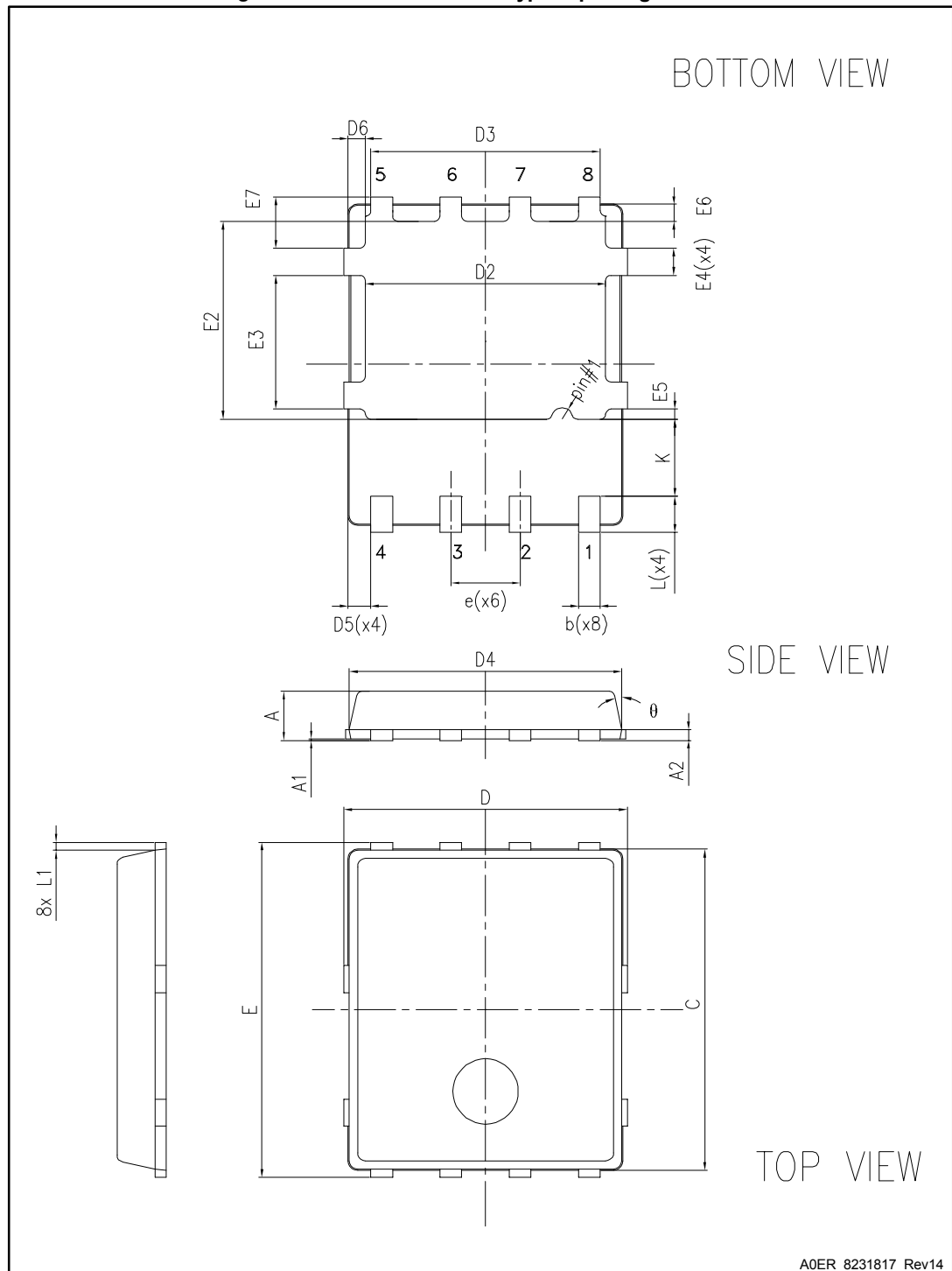
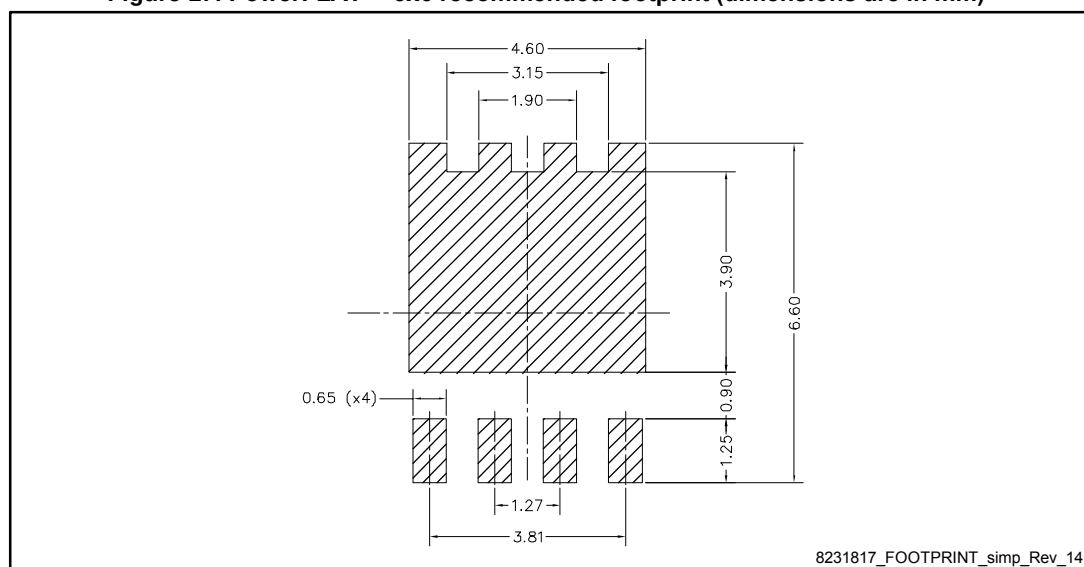


Table 9: PowerFLAT™ 5x6 type R mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.20
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.20
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
e		1.27	
E	5.95	6.15	6.35
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.75	0.90	1.05
K	1.275		1.575
L	0.60		0.80
L1	0.05	0.15	0.25
θ		0°	12°

Figure 17: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



5 Packing information

Figure 18: PowerFLAT™ 5x6 tape (dimensions are in mm)

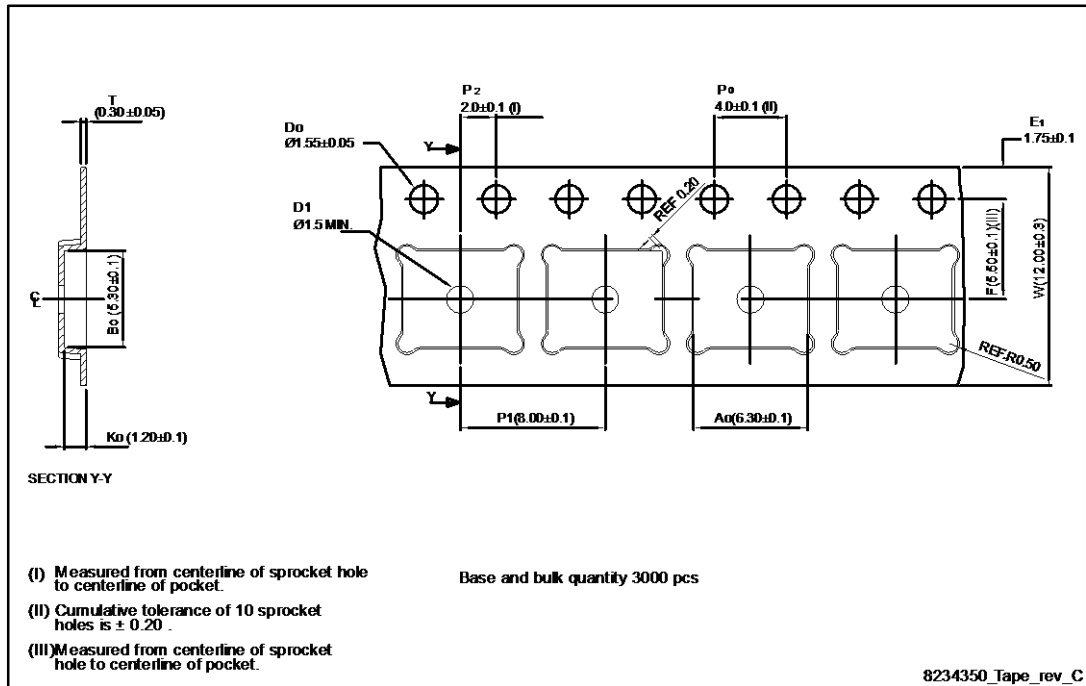
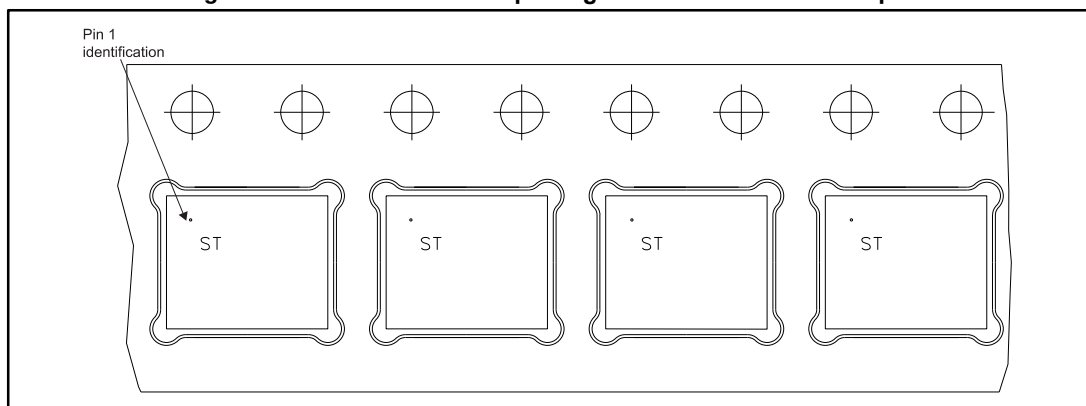


Figure 19: PowerFLAT™ 5x6 package orientation in carrier tape



Technical drawing of a reel tape carrier, showing dimensions in millimeters.

Top View (Left): Circular carrier with a central hole. Dimensions include: PART NO. (label), R25.00 (radius), $\phi 4.00$ (central hole), $\phi 2.50$ (inner hole), and $\sqrt{2} \phi A$ (diagonal dimension).

Top View (Right): Circular carrier with a central hole. Dimensions include: A (overall diameter), 330 (+0/-4.0) (overall diameter), and ESD LOGO (label).

Side View (Center): Shows the profile of the carrier. Dimensions include: W3 11.9/15.4, W2 18.4 (max), 2N 178(± 2), and W1 12.4 (+2/-0).

Core Detail (Bottom Left): Circular detail of the core. Dimensions include: R1.10 (radius), $\phi 21.2$ (outer diameter), $\phi 13.00$ (inner diameter), and 2.20 (width).

Notes:

- All dimensions are in millimeters.
- ESD LOGO (Electrostatic Discharge Protection) is indicated on the right side view.

6 Revision history

Table 10: Document revision history

Date	Revision	Changes
30-May-2014	1	First release.
05-Sep-2014	2	Updated the title, the features and the description in cover page. Updated Section 7: " <i>Electrical characteristics</i> ". Minor text changes.
11-Sep-2014	3	Updated Figure 6: " <i>Gate charge vs gate-source voltage</i> ". Minor text changes.
16-Dec-2014	4	Document status promoted from preliminary to production data.
07-Apr-2015	5	Updated Section 7.1: " <i>Electrical characteristics (curves)</i> " and Section 9.1: " <i>PowerFLAT 5x6 type R package information</i> "
20-Oct-2016	6	Updated Figure 2: "Safe operating area" . Minor text changes.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2016 STMicroelectronics – All rights reserved