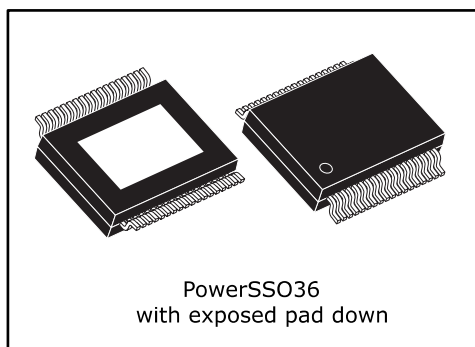


## 45 W + 45 W dual BTL class-D audio amplifier

Datasheet - production data



### Features

- Wide-range single-supply operation (7 - 26 V)
- Possible output configurations:
  - 2 x PBTL
  - 1 x Parallel BTL
- BTL output capabilities ( $V_{CC} = 22\text{ V}$ ):
  - 44 W + 44 W, 4  $\Omega$ , THD 1%
  - 57 W + 57 W, 4  $\Omega$ , THD 10%
  - 32 W + 32 W, 6  $\Omega$ , THD 1%
  - 41 W + 41 W, 6  $\Omega$ , THD 10%
  - 25 W + 25 W, 8  $\Omega$ , THD 1%
  - 32 W + 32 W, 8  $\Omega$ , THD 10%
- Parallel BTL output capabilities ( $V_{CC} = 22\text{ V}$ ):
  - 70 W, 3  $\Omega$ , THD 1%
  - 90 W, 3  $\Omega$ , THD 10%
- High efficiency

- Four selectable, fixed-gain settings of nominally 20.8 dB, 26.8 dB, 30 dB and 32.8 dB
- Differential inputs minimize common-mode noise
- Standby, mute and play operating modes
- Short-circuit protection
- Output power limited by  $P_{LIMIT}$  function
- Detection of shorted output pins during startup
- Thermal overload protection
- ECOPACK® environmentally friendly package

### Description

The TDA7492PE is a dual BTL class-D audio amplifier with single power supply designed for home audio applications.

The device is housed in a 36-pin PowerSSO package with exposed pad down (EPD) to facilitate power dissipation through a properly designed PCB area underneath the TDA7492PE.

**Table 1: Device summary**

| Order code  | Operating temp. range | Package         | Packaging     |
|-------------|-----------------------|-----------------|---------------|
| TDA7492PE   | -40 to +85°C          | PowerSSO-36 EPD | Tube          |
| TDA7492PETR |                       |                 | Tape and reel |

---

## Contents

|          |                                         |           |
|----------|-----------------------------------------|-----------|
| <b>1</b> | <b>Device block diagram.....</b>        | <b>5</b>  |
| <b>2</b> | <b>Pin description .....</b>            | <b>6</b>  |
| 2.1      | Pinout.....                             | 6         |
| 2.2      | Pin list .....                          | 7         |
| <b>3</b> | <b>Electrical specifications.....</b>   | <b>8</b>  |
| 3.1      | Absolute maximum ratings.....           | 8         |
| 3.2      | Thermal data.....                       | 8         |
| 3.3      | Electrical specifications .....         | 9         |
| 3.4      | Stereo BTL application.....             | 10        |
| 3.5      | Parallel BTL (mono) application .....   | 10        |
| <b>4</b> | <b>Application information .....</b>    | <b>11</b> |
| 4.1      | Gain setting.....                       | 11        |
| 4.2      | Stereo and mono applications.....       | 11        |
| 4.3      | Smart protections .....                 | 11        |
| 4.3.1    | Overcurrent protection (OCP) .....      | 11        |
| 4.3.2    | Thermal protection.....                 | 12        |
| 4.3.3    | Power limit .....                       | 12        |
| 4.4      | Mode selection.....                     | 13        |
| <b>5</b> | <b>Schematic diagram.....</b>           | <b>15</b> |
| <b>6</b> | <b>Characterization curves.....</b>     | <b>17</b> |
| <b>7</b> | <b>Package information .....</b>        | <b>19</b> |
| 7.1      | PowerSSO36 EPD package information..... | 19        |
| <b>8</b> | <b>Revision history .....</b>           | <b>22</b> |

## List of tables

|                                                                               |    |
|-------------------------------------------------------------------------------|----|
| Table 1: Device summary .....                                                 | 1  |
| Table 2: Pin description list .....                                           | 7  |
| Table 3: Absolute maximum ratings .....                                       | 8  |
| Table 4: Thermal data .....                                                   | 8  |
| Table 5: Electrical specifications .....                                      | 9  |
| Table 6: Stereo BTL application .....                                         | 10 |
| Table 7: Stereo BTL (mono) application .....                                  | 10 |
| Table 8: Gain settings .....                                                  | 11 |
| Table 9: Overcurrent protection .....                                         | 11 |
| Table 10: Overcurrent protection (mute mode) .....                            | 12 |
| Table 11: Max effective voltage of PLIMIT pin vs. power supply and load ..... | 13 |
| Table 12: Mode settings .....                                                 | 13 |
| Table 13: BTL configuration .....                                             | 16 |
| Table 14: PowerSSO-36 EPD package mechanical data .....                       | 21 |
| Table 15: Document revision history .....                                     | 22 |

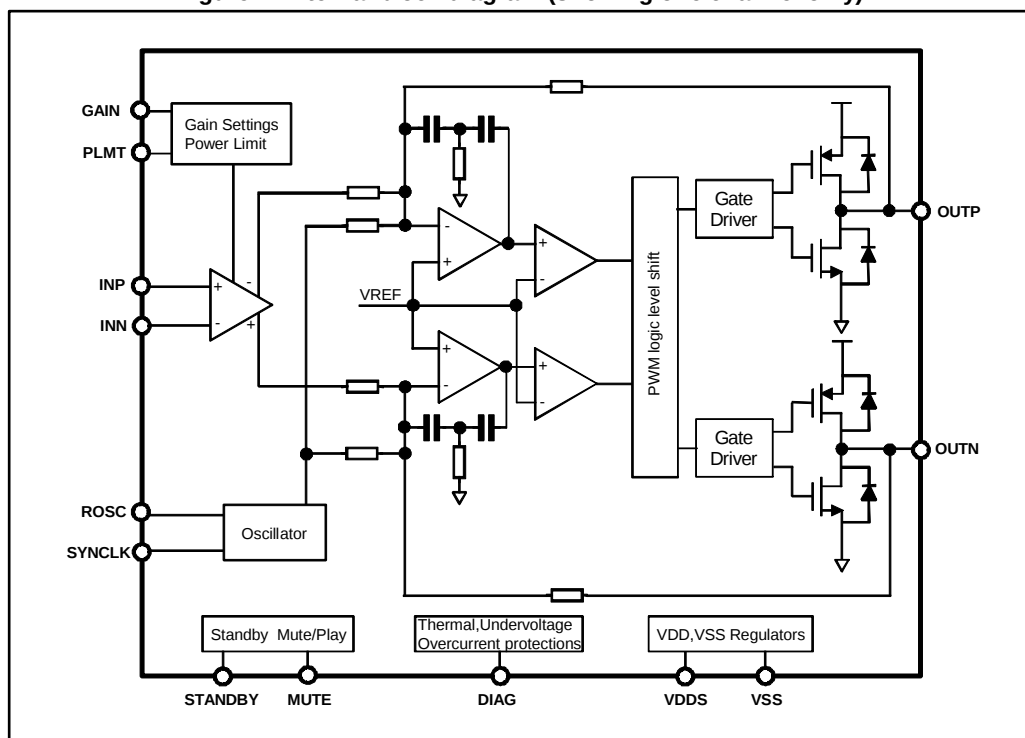
## List of figures

|                                                                   |    |
|-------------------------------------------------------------------|----|
| Figure 1: Internal block diagram (showing one channel only) ..... | 5  |
| Figure 2: Pin connections (top view, PCB view) .....              | 6  |
| Figure 3: Mono BTL settings.....                                  | 11 |
| Figure 4: Recommended power limit pin connections.....            | 12 |
| Figure 5: Standby and mute circuits .....                         | 14 |
| Figure 6: Turn-on/off sequence for minimizing speaker “pop” ..... | 14 |
| Figure 7: Application circuit.....                                | 15 |
| Figure 8: Output power vs. supply voltage .....                   | 17 |
| Figure 9: Efficiency vs. output power .....                       | 17 |
| Figure 10: THD vs. output power (f = 1 kHz) .....                 | 17 |
| Figure 11: THD vs. output power (100 Hz).....                     | 17 |
| Figure 12: THD vs. frequency .....                                | 17 |
| Figure 13: Frequency response.....                                | 17 |
| Figure 14: FFT (0 dB) .....                                       | 18 |
| Figure 15: FFT (-60 dB) .....                                     | 18 |
| Figure 16: PSRR parameter .....                                   | 18 |
| Figure 17: PowerSSO-36 EPD package outline.....                   | 20 |

# 1 Device block diagram

Figure 1: "Internal block diagram (showing one channel only)" shows the block diagram of one of the two identical channels of the TDA7492PE.

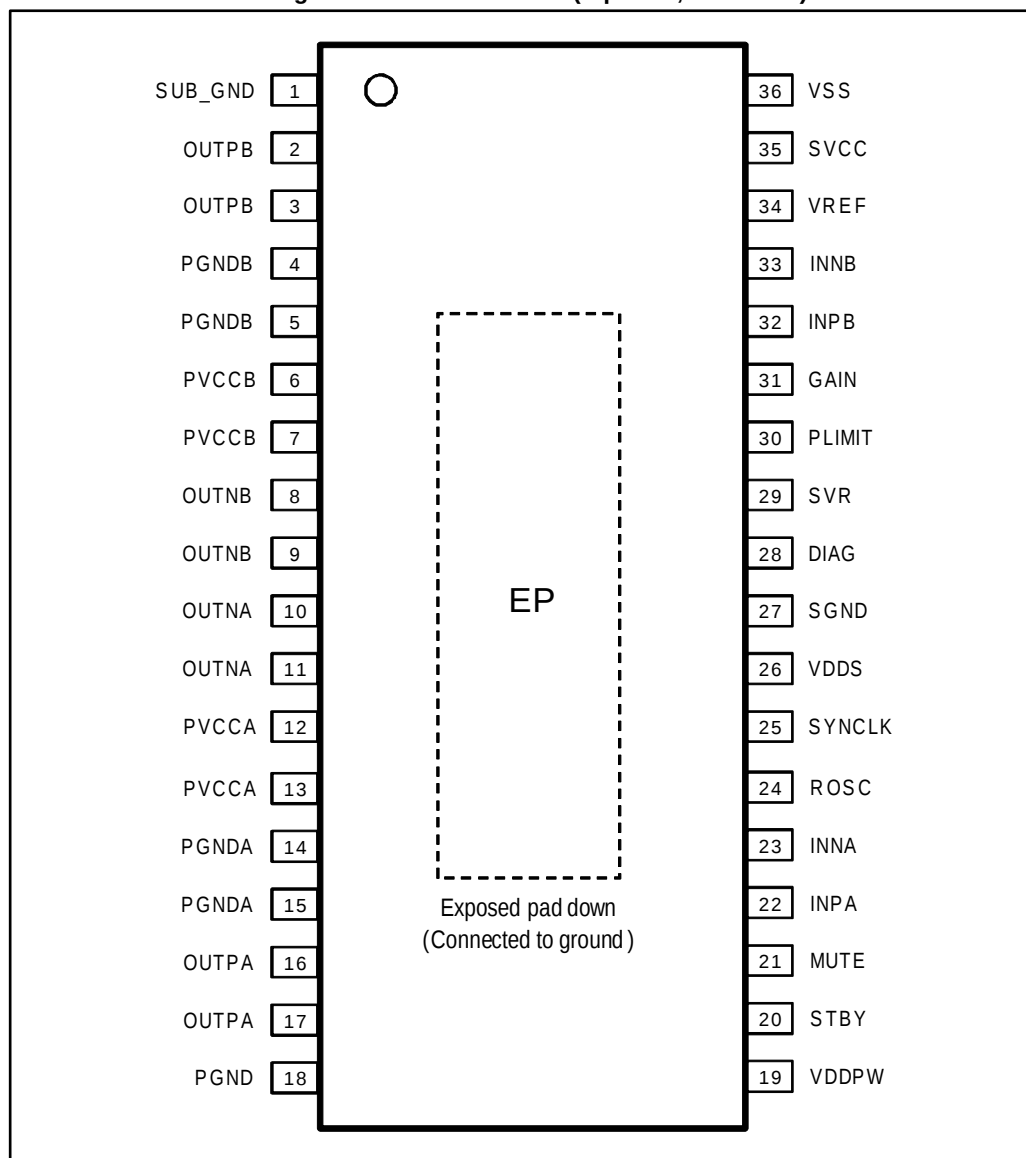
Figure 1: Internal block diagram (showing one channel only)



## 2 Pin description

### 2.1 Pinout

Figure 2: Pin connections (top view, PCB view)



## 2.2 Pin list

Table 2: Pin description list

| Number | Name    | Type | Description                                                           |
|--------|---------|------|-----------------------------------------------------------------------|
| 1      | SUB_GND | PWR  | Connect to the frame                                                  |
| 2, 3   | OUTPB   | O    | Positive PWM for right channel                                        |
| 4, 5   | PGNDB   | PWR  | Power stage ground for right channel                                  |
| 6, 7   | PVCCB   | PWR  | Power supply for right channel                                        |
| 8, 9   | OUTNB   | O    | Negative PWM output for right channel                                 |
| 10, 11 | OUTNA   | O    | Negative PWM output for left channel                                  |
| 12, 13 | PVCCA   | PWR  | Power supply for left channel                                         |
| 14, 15 | PGNDA   | PWR  | Power stage ground for left channel                                   |
| 16, 17 | OUTPA   | O    | Positive PWM output for left channel                                  |
| 18     | PGND    | PWR  | Power stage ground                                                    |
| 19     | VDDPW   | O    | 3.3 V (nominal) regulator output referred to ground for power stage   |
| 20     | STBY    | I    | Standby mode control                                                  |
| 21     | MUTE    | I    | Mute mode control                                                     |
| 22     | INPA    | I    | Positive differential input of left channel                           |
| 23     | INNA    | I    | Negative differential input of left channel                           |
| 24     | ROSC    | O    | Master oscillator frequency-setting pin                               |
| 25     | SYNCLK  | I/O  | Clock in/out for external oscillator                                  |
| 26     | VDDS    | O    | 3.3 V (nominal) regulator output referred to ground for signal blocks |
| 27     | SGND    | PWR  | Signal ground                                                         |
| 28     | DIAG    | O    | Open-drain diagnostic output                                          |
| 29     | SVR     | O    | Supply voltage rejection                                              |
| 30     | PLIMIT  | I    | Output voltage level setting                                          |
| 31     | GAIN    | I    | Gain setting input                                                    |
| 32     | INPB    | I    | Positive differential input of right channel                          |
| 33     | INNB    | I    | Negative differential input of right channel                          |
| 34     | VREF    | O    | Half VDDS (nominal) referred to ground                                |
| 35     | SVCC    | PWR  | Signal power supply                                                   |
| 36     | VSS     | O    | 3.3 V (nominal) regulator output referred to power supply             |
| -      | EP      | -    | Exposed pad for heatsink, to be connected to GND                      |

## 3 Electrical specifications

### 3.1 Absolute maximum ratings

Table 3: Absolute maximum ratings

| Symbol           | Parameter                                                                    | Value        | Unit |
|------------------|------------------------------------------------------------------------------|--------------|------|
| V <sub>CC</sub>  | DC supply voltage for pins PVCCA, PVCCB, SVCC                                | 30           | V    |
| V <sub>I</sub>   | Voltage limits for input pins STBY, MUTE, INNA, INPA, INNB, INPB, GAIN, MODE | -0.3 to +4.6 | V    |
| T <sub>j</sub>   | Operating junction temperature                                               | -40 to +150  | °C   |
| T <sub>op</sub>  | Operating ambient temperature                                                | -40 to +85   | °C   |
| T <sub>stg</sub> | Storage temperature                                                          | -40 to +150  | °C   |

### 3.2 Thermal data

Table 4: Thermal data

| Symbol                 | Parameter                               | Min. | Typ. | Max. | Unit |
|------------------------|-----------------------------------------|------|------|------|------|
| R <sub>th j-case</sub> | Thermal resistance, junction-to-case    | -    | 2.98 |      | °C/W |
| R <sub>th j-amb</sub>  | Thermal resistance, junction-to-ambient |      | 24   |      | °C/W |

### 3.3 Electrical specifications

Unless otherwise stated, the results in below are given for the conditions:  $V_{CC} = 22\text{ V}$ ,  $R_L = 6\ \Omega$ ,  $R_{OSC} = R_3 = 33\text{ k}\Omega$ ,  $f = 1\text{ kHz}$ ,  $G_V = 20.8\text{ dB}$  and  $T_{amb} = 25\text{ }^\circ\text{C}$ .

Table 5: Electrical specifications

| Symbol                          | Parameter                                                 | Condition                                                            | Min.    | Typ. | Max. | Unit |
|---------------------------------|-----------------------------------------------------------|----------------------------------------------------------------------|---------|------|------|------|
| V <sub>CC</sub>                 | Supply voltage for pins PVCCA, PVCCB, SVCC                | -                                                                    | 7       | -    | 26   | V    |
| I <sub>q</sub>                  | Total quiescent current                                   | No LC filter, no load                                                | -       | 40   |      | mA   |
| I <sub>qSTBY</sub>              | Quiescent current in standby                              | -                                                                    | -       | 1    | -    | μA   |
| V <sub>OS</sub>                 | Output offset voltage                                     | V <sub>i</sub> = 0, no load                                          |         | 20   |      | mV   |
| I <sub>OCP</sub>                | Overcurrent protection threshold to switch off the device |                                                                      | 9       | 10   | 13   | A    |
| T <sub>j</sub>                  | Junction temperature at thermal shutdown                  | -                                                                    | 140     | 150  | 160  | °C   |
| R <sub>i</sub>                  | Input resistance                                          | Differential input                                                   |         | 60   | -    | kΩ   |
| R <sub>dsON</sub>               | Power transistor on-resistance                            | High side                                                            | -       | 0.2  | -    | Ω    |
|                                 |                                                           | Low side                                                             | -       | 0.2  | -    |      |
| G <sub>V</sub>                  | Closed-loop gain                                          | GAIN < 0.25*Vdd                                                      |         | 20.8 | -    | dB   |
|                                 |                                                           | 0.25*Vdd < GAIN < 0.5*Vdd                                            | -       | 26.8 | -    |      |
|                                 |                                                           | 0.5*Vdd < GAIN < 0.75*Vdd                                            | -       | 30   | -    |      |
|                                 |                                                           | GAIN1 > 0.75*Vdd                                                     | -       | 32.8 | -    |      |
| ΔG <sub>V</sub>                 | Gain matching                                             | -                                                                    |         | -    | ±1   | dB   |
| CT                              | Cross talk                                                | f = 1 kHz, P <sub>O</sub> = 1 W                                      |         | 70   | -    | dB   |
| SVRR                            | Supply voltage rejection ratio                            | fr = 100 Hz, Vr = 0.5 Vpp, C <sub>SVR</sub> = 10 μF                  | -       | 60   | -    | dB   |
| T <sub>r</sub> , T <sub>f</sub> | Rise and fall times                                       | -                                                                    | -       | 24   | 40   | ns   |
| f <sub>sw</sub>                 | Switching frequency                                       | Internal oscillator                                                  |         | 500  |      | kHz  |
| f <sub>SWR</sub>                | Output switching frequency range                          | With internal oscillator by changing R <sub>osc</sub> <sup>(1)</sup> | 450     | -    | 550  | kHz  |
| V <sub>inH</sub>                | Digital input high (H)                                    | -                                                                    | 2.0     | -    | -    | V    |
| V <sub>inL</sub>                | Digital input low (L)                                     |                                                                      | -       | -    | 0.8  |      |
| Function mode                   | Standby, Mute, Play                                       | STBY < 0.5 V Mute = X                                                | Standby |      |      |      |
|                                 |                                                           | STBY > 2.5 V Mute < 0.8 V                                            | Mute    |      |      |      |
|                                 |                                                           | STBY > 2.5 V Mute > 2.5 V                                            | Play    |      |      |      |
| A <sub>MUTE</sub>               | Mute attenuation                                          | V <sub>MUTE</sub> = 1 V                                              | 60      | 80   | -    | dB   |

**Notes:**

<sup>(1)</sup> $f_{sw} = 10^6 / [(R_{osc} \cdot 12 + 110) \cdot 4]\text{ kHz}$ ,  $f_{SYNCLK} = 2 \cdot f_{sw}$  (where  $R_{osc}$  is in k $\Omega$ . and  $f_{sw}$  in kHz) with  $R_{osc} = 33\text{ k}\Omega$ .

### 3.4 Stereo BTL application

All specifications are for  $V_{CC} = 22\text{ V}$ ,  $R_{osc} = 33\text{ k}\Omega$ ,  $f = 1\text{ kHz}$ ,  $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified.

Table 6: Stereo BTL application

| Symbol | Parameter                 | Condition                                                               | Min. | Typ. | Max. | Unit          |
|--------|---------------------------|-------------------------------------------------------------------------|------|------|------|---------------|
| $P_o$  | Output power              | $R_L = 6\text{ }\Omega$ , THD = 10%                                     | -    | 41   | -    | W             |
|        |                           | $R_L = 6\text{ }\Omega$ , THD = 1%                                      | -    | 32   | -    |               |
|        |                           | $R_L = 6\text{ }\Omega$ , THD = 10%,<br>$V_{CC} = 18\text{ V}$          | -    | 27   | -    |               |
|        |                           | $R_L = 6\text{ }\Omega$ , THD = 1%,<br>$V_{CC} = 18\text{ V}$           | -    | 21   | -    |               |
| THD    | Total harmonic distortion | $P_o = 1\text{ W}$ , $f_{in} = 1\text{ kHz}$                            | -    | 0.04 | -    | %             |
| VN     | Total output noise        | Inputs shorted and connected to GND,<br>A Curve, $G_v = 20.8\text{ dB}$ | -    | 150  | -    | $\mu\text{V}$ |

### 3.5 Parallel BTL (mono) application

All specifications are for  $V_{CC} = 22\text{ V}$ ,  $R_{osc} = 33\text{ k}\Omega$ ,  $f = 1\text{ kHz}$ ,  $T_{amb} = 25\text{ }^{\circ}\text{C}$ , INPB, INNBB connected to VDDS, unless otherwise specified.

Table 7: Stereo BTL (mono) application

| Symbol | Parameter                 | Condition                                                               | Min. | Typ. | Max. | Unit          |
|--------|---------------------------|-------------------------------------------------------------------------|------|------|------|---------------|
| $P_o$  | Output power              | $R_L = 3\text{ }\Omega$ , THD = 10%                                     | -    | 90   | -    | W             |
|        |                           | $R_L = 3\text{ }\Omega$ , THD = 1%                                      | -    | 70   | -    |               |
|        |                           | $R_L = 3\text{ }\Omega$ , THD = 10%,<br>$V_{CC} = 18\text{ V}$          | -    | 53   | -    |               |
|        |                           | $R_L = 3\text{ }\Omega$ , THD = 1%,<br>$V_{CC} = 18\text{ V}$           | -    | 41   | -    |               |
| THD    | Total harmonic distortion | $P_o = 1\text{ W}$ , $f_{in} = 1\text{ kHz}$                            | -    | 0.04 | -    | %             |
| VN     | Total output noise        | Inputs shorted and connected to GND,<br>A Curve, $G_v = 20.8\text{ dB}$ | -    | 150  | -    | $\mu\text{V}$ |

## 4 Application information

### 4.1 Gain setting

The four gain settings of the TDA7492PE are set by GAIN (pin 31). Internally, gain is set by changing the feedback resistors of the amplifier. The gain setting pins can be controlled by standard logic drivers.

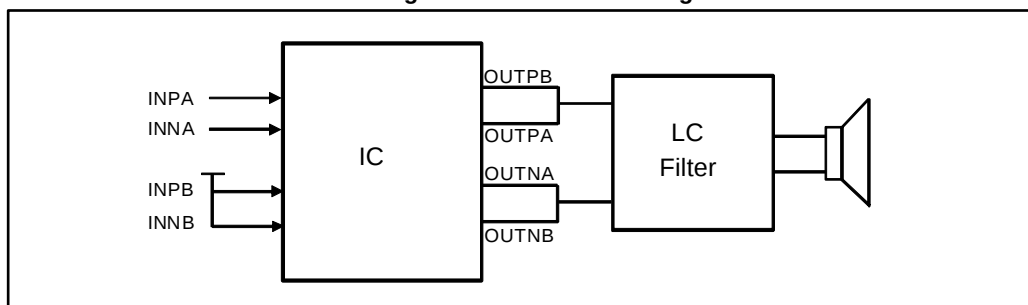
Table 8: Gain settings

| Voltage on GAIN pin                                                      | Total gain | Application recommendations       |
|--------------------------------------------------------------------------|------------|-----------------------------------|
| $V_{\text{GAIN}} < 0.25 \cdot V_{\text{DD}}S$                            | 20.8 dB    | GAIN pin connected to SGND        |
| $0.25 \cdot V_{\text{DD}}S < V_{\text{GAIN}} < 0.5 \cdot V_{\text{DD}}S$ | 26.8 dB    | External resistor divider < 100 k |
| $0.5 \cdot V_{\text{DD}}S < V_{\text{GAIN}} < 0.75 \cdot V_{\text{DD}}S$ | 30 dB      | External resistor divider < 100 k |
| $V_{\text{GAIN}} > 0.75 \cdot V_{\text{DD}}S$                            | 32.8 dB    | GAIN pin connected to VDD         |

### 4.2 Stereo and mono applications

The TDA7492PE can be used in stereo BTL or in mono BTL configuration. When the input pins, INPB and INNB of the right channel are directly shorted to VDD (without input capacitors) the device is in mono configuration as shown in [Figure 3: "Mono BTL settings"](#).

Figure 3: Mono BTL settings



### 4.3 Smart protections

#### 4.3.1 Overcurrent protection (OCP)

If the overcurrent protection threshold is reached, the power stage will be shut down immediately. The device will recover automatically when the fault is removed.

Table 9: Overcurrent protection

|               | I (Shutdown) |
|---------------|--------------|
| High side (A) | 11.2         |
| Low side (A)  | 10.0         |

The thresholds in mute mode are reduced to about 1/2 and two typical thresholds are as follows.

**Table 10: Overcurrent protection (mute mode)**

|               | I (Shutdown) |
|---------------|--------------|
| High side (A) | 6.2          |
| Low side (A)  | 5.9          |

### 4.3.2 Thermal protection

When internal die temperature exceeds 140 °C, the device enters into Mute by pulling the MUTE pin low first.

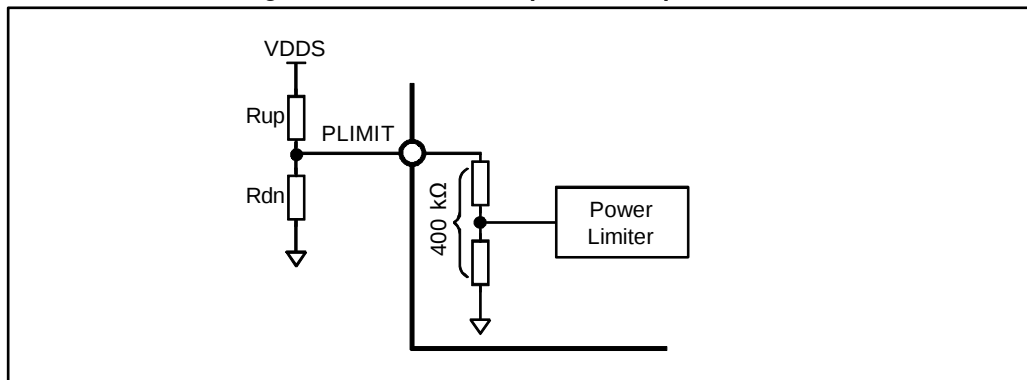
When internal die temperature exceeds 150 °C, the device directly shuts down the power stage. The TDA7492PE automatically recovers when the temperature become lower than the threshold.

### 4.3.3 Power limit

A built-in power limit is used to limit the output voltage level below the supply rail by limiting the duty cycle. The limit level is set through the voltage at PLIMIT (pin 30). The pin voltage is set by the following equation:

$$V_{PLIMIT} = V_{DD} \left[ \frac{(R_{dn}/400k)}{(R_{dn}/400k + R_{up})} \right]$$

**Figure 4: Recommended power limit pin connections**



It is recommended that external resistors are less than 40 kΩ if a voltage divider is used as shown in [Figure 4: "Recommended power limit pin connections"](#). The relationship of the maximum duty cycle ( $D_{max}$ ) and the voltage at  $P_{LIMIT}$  is:

$$D_{max} = \frac{\left\{ 8.8 \times \frac{V_{PLIMIT}}{V_{cc} - \frac{2 \times V_{cc} \times R_s}{R_{load} \times 2 \times R_s}} + 1 \right\}}{2}$$

Where  $V_{CC}$  is the power supply voltage,  $V_{PLIMIT}$  is the voltage applied at the  $P_{LIMIT}$  pin,  $R_s$  is the series resistance including  $R_{ds(on)}$  of the power transistor, output filter resistance and bonding wire resistance.  $R_{load}$  is the load resistance.

An example of maximum effective control voltage at  $P_{LIMIT}$  vs. power supply and load resistance is shown in [Table 11: "Max effective voltage of PLIMIT pin vs. power supply and load"](#).

**Table 11: Max effective voltage of PLIMIT pin vs. power supply and load**

| Rload      | Power supply |        |        |
|------------|--------------|--------|--------|
|            | 7 V          | 13 V   | 24 V   |
| 4 $\Omega$ | 0.71 V       | 1.32 V | 2.44 V |
| 6 $\Omega$ | 0.74 V       | 1.37 V | 2.53 V |
| 8 $\Omega$ | 0.75 V       | 1.39 V | 2.57 V |

## 4.4 Mode selection

The three operating modes of the TDA7492PE are set by two inputs: STBY (pin 20) and MUTE (pin 21).

- Standby mode: all circuits are turned off, very low current consumption.
- Mute mode: inputs are connected to ground and the positive and negative PWM outputs are at 50% duty cycle
- Play mode: the amplifiers are active.

The protection functions of the TDA7492PE are implemented by pulling down the voltages of the STBY and MUTE inputs shown in [Figure 5: "Standby and mute circuits"](#). The input current of the corresponding pins must be limited to 200  $\mu$ A.

**Table 12: Mode settings**

| Mode    | STBY             | MUTE           |
|---------|------------------|----------------|
| Standby | L <sup>(1)</sup> | X (don't care) |
| Mute    | H                | L              |
| Play    | H                | H              |

**Notes:**

<sup>(1)</sup>Drive levels defined in [Table 5: "Electrical specifications"](#).

Figure 5: Standby and mute circuits

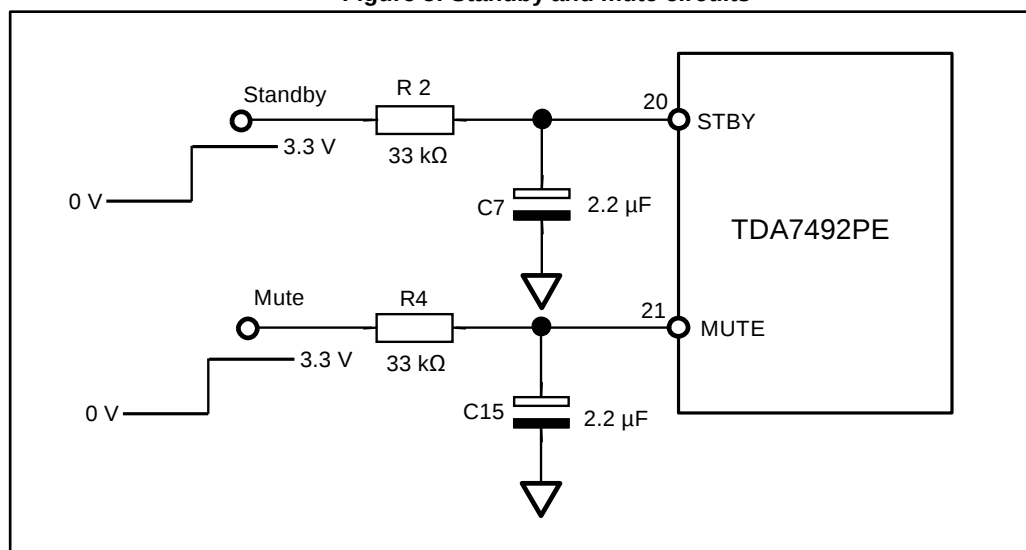
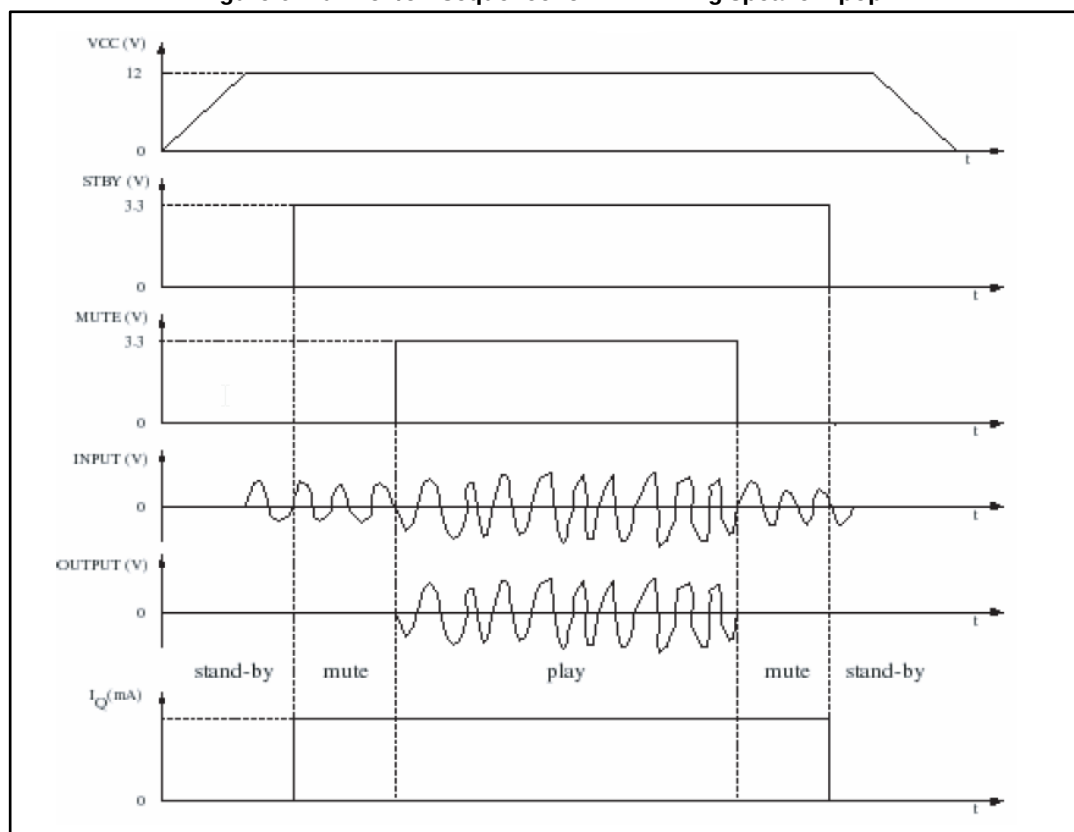


Figure 6: Turn-on/off sequence for minimizing speaker “pop”



5 Schematic diagram

Figure 7: Application circuit

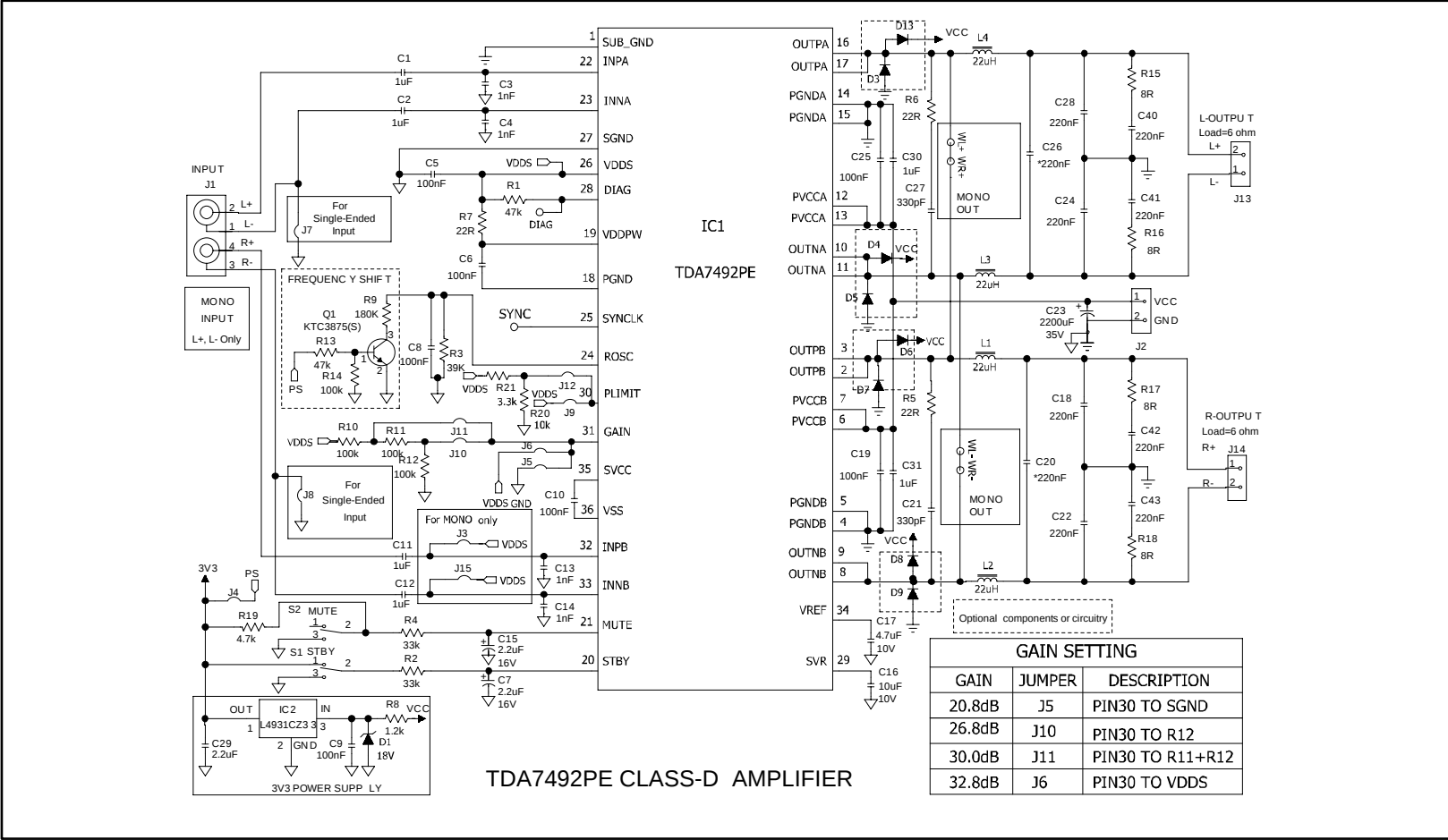


Table 13: BTL configuration

| Load impedance | L4, L3, L2, L1 | C26, C20  | C28, C24, C22, C18 | R15, R16, R17, R18 | C40, C41, C42, C43 |
|----------------|----------------|-----------|--------------------|--------------------|--------------------|
| 4 $\Omega$     | 15 $\mu$ h     | 1 $\mu$ F | 220 nF             | 8 $\Omega$         | 220 nF             |
| 6 $\Omega$     | 22 $\mu$ h     | 680 nF    | 220 nF             | 8 $\Omega$         | 220 nF             |
| 8 $\Omega$     | 22 $\mu$ h     | 470 nF    | 220 nF             | 8 $\Omega$         | 220 nF             |

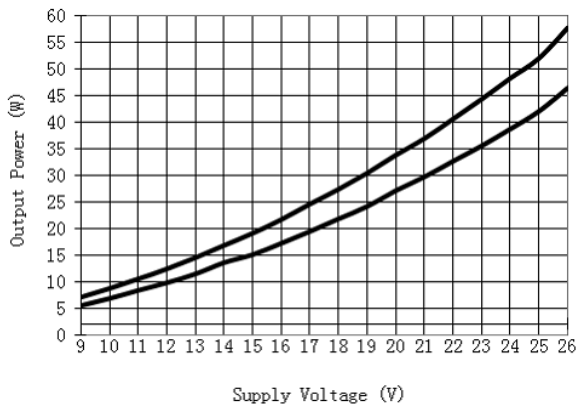
## 6 Characterization curves

Unless otherwise stated, measurements were made under the following conditions:

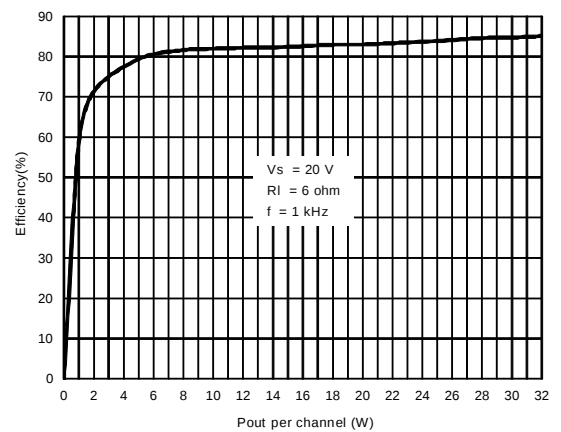
$V_{CC} = 22\text{ V}$ ,  $R_I = 6\ \Omega$ ,  $f = 1\text{ kHz}$ ,  $G_v = 20.8\text{ dB}$ ,  $R_{osc} = 33\text{ k}\Omega$ , Gain = 20.8 dB and  $T_{amb} = 25\text{ }^\circ\text{C}$ .

*Note: Maximum output power must be derated according to case temperature.*

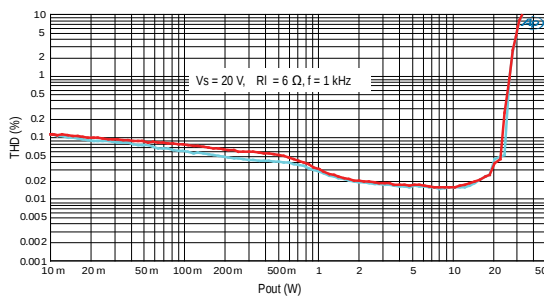
**Figure 8: Output power vs. supply voltage**



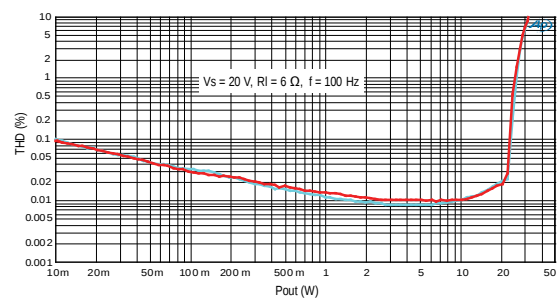
**Figure 9: Efficiency vs. output power**



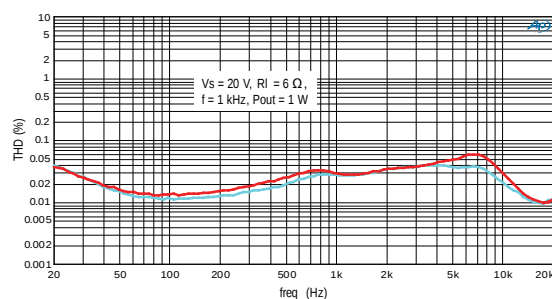
**Figure 10: THD vs. output power (f = 1 kHz)**



**Figure 11: THD vs. output power (100 Hz)**



**Figure 12: THD vs. frequency**



**Figure 13: Frequency response**

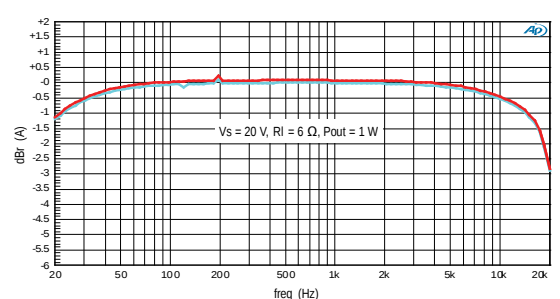


Figure 14: FFT (0 dB)

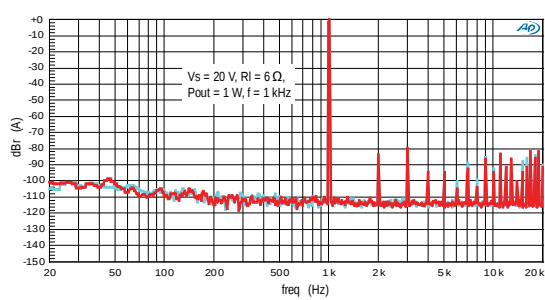


Figure 15: FFT (-60 dB)

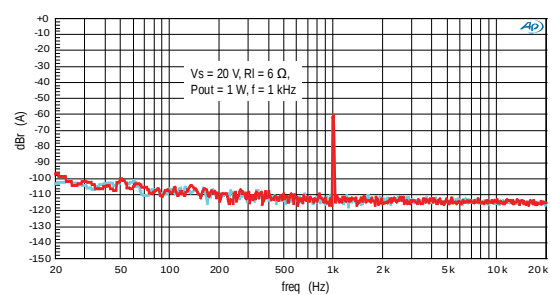
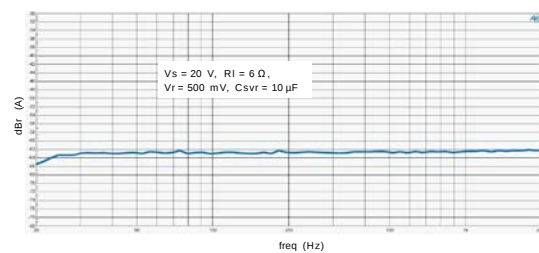


Figure 16: PSRR parameter



## 7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 7.1 PowerSSO36 EPD package information

The TDA7492PE comes in a 36-pin PowerSSO package with exposed pad down (EPD).

*Figure 17: "PowerSSO-36 EPD package outline"* shows the package outline and *Table 14: "PowerSSO-36 EPD package mechanical data"* gives the dimensions.

Figure 17: PowerSSO-36 EPD package outline

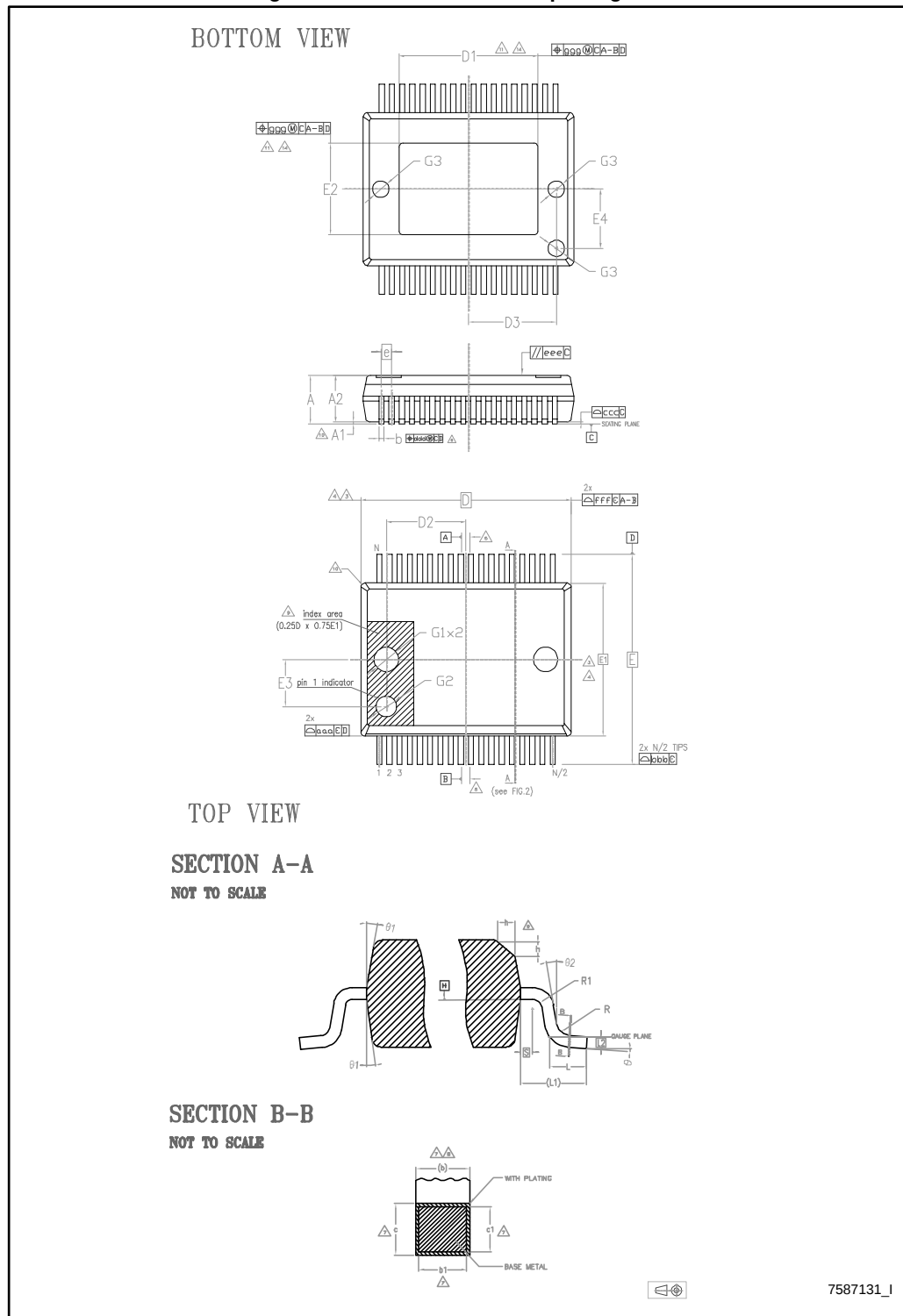


Table 14: PowerSSO-36 EPD package mechanical data

| Symbol | Dimensions in mm |      |      | Dimensions in inches |       |       |
|--------|------------------|------|------|----------------------|-------|-------|
|        | Min.             | Typ. | Max. | Min.                 | Typ.  | Max.  |
| θ      | 0°               | -    | 8°   | 0°                   | -     | 8°    |
| θ1     | 5°               | -    | 10°  | 5°                   | -     | 10°   |
| θ2     | 0°               | -    | -    | 0°                   | -     | -     |
| A      | 2.15             | -    | 2.45 | 0.085                | -     | 0.096 |
| A1     | 0.00             | -    | 0.10 | 0.00                 | -     | 0.004 |
| A2     | 2.15             | -    | 2.35 | 0.085                | -     | 0.093 |
| b      | 0.18             | -    | 0.32 | 0.007                | -     | 0.013 |
| b1     | 0.13             | 0.25 | 0.30 | 0.005                | 0.010 | 0.012 |
| c      | 0.23             | -    | 0.32 | 0.009                | -     | 0.013 |
| c1     | 0.20             | 0.20 | 0.30 | 0.008                | 0.008 | 0.012 |
| D      | 10.30 BSC        |      |      | 0.406 BSC            |       |       |
| D1     | 6.50             | -    | 7.10 | 0.256                | -     | 0.280 |
| D2     | -                | 3.65 | -    | -                    | 0.144 | -     |
| D3     | -                | 4.30 | -    | -                    | 0.169 | -     |
| e      | 0.50 BSC         |      |      | 0.020 BSC            |       |       |
| E      | 10.30 BSC        |      |      | 0.406 BSC            |       |       |
| E1     | 7.50 BSC         |      |      | 0.295 BSC            |       |       |
| E2     | 4.10             | -    | 4.70 | 0.161                | -     | 0.185 |
| E3     | -                | 2.30 | -    | -                    | 0.091 | -     |
| E4     | -                | 2.90 | -    | -                    | 0.114 | -     |
| G1     | -                | 1.20 | -    | -                    | 0.047 | -     |
| G2     | -                | 1.00 | -    | -                    | 0.039 | -     |
| G3     | -                | 0.80 | -    | -                    | 0.032 | -     |
| h      | 0.30             | -    | 0.40 | 0.012                | -     | 0.016 |
| L      | 0.55             | 0.70 | 0.85 | 0.022                | 0.028 | 0.033 |
| L1     | 1.40 REF         |      |      | 0.055 REF            |       |       |
| L2     | 0.25 BSC         |      |      | 0.010 BSC            |       |       |
| N      | 36               |      |      |                      |       |       |
| R      | 0.30             | -    | -    | 0.012                | -     | -     |
| R1     | 0.20             | -    | -    | 0.008                | -     | -     |
| S      | 0.25             | -    | -    | 0.010                | -     | -     |

## 8 Revision history

**Table 15: Document revision history**

| Date        | Revision | Changes                                                                                                                                                                                                                                                 |
|-------------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 14-Nov-2014 | 1        | Initial release                                                                                                                                                                                                                                         |
| 24-Feb-2017 | 2        | Updated minimum voltage to 7 V throughout datasheet<br>Updated V <sub>OS</sub> and T <sub>r</sub> , T <sub>f</sub> in <a href="#">Table 5: "Electrical specifications"</a><br>Updated <a href="#">Section 7.1: "PowerSSO36 EPD package information"</a> |

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