SC644

Light Management Unit with 4 LDOs and SemPulse® Interface

POWER MANAGEMENT

Features

- Input supply voltage range — 2.9V to 5.5V
- Very high efficiency charge pump driver system with three modes — 1x, 1.5x, and 2x
- Six programmable current sinks with 29 increments from 0mA to 25mA
- Four programmable 200mA low-noise LDO regulators
- Programmable driver configurations for main and sub-display backlight
- Fade-in/fade-out feature for main and sub display backlight
- SemPulse single wire interface
- Backlight current accuracy — ±1.5% typical
- Backlight current matching — ±0.5% typical
- Automatic sleep mode with LEDs off
- Shutdown current — 0.1µA typical
- Ultra-thin package — 3 x 3 x 0.6 (mm)
- Lead free and halogen free
- WEEE and RoHS compliant

Applications

- Cellular phones, smart phones, and PDAs
- LCD display modules
- Portable media players
- Digital cameras and GPS units
- Display backlighting and LED indicators

Description

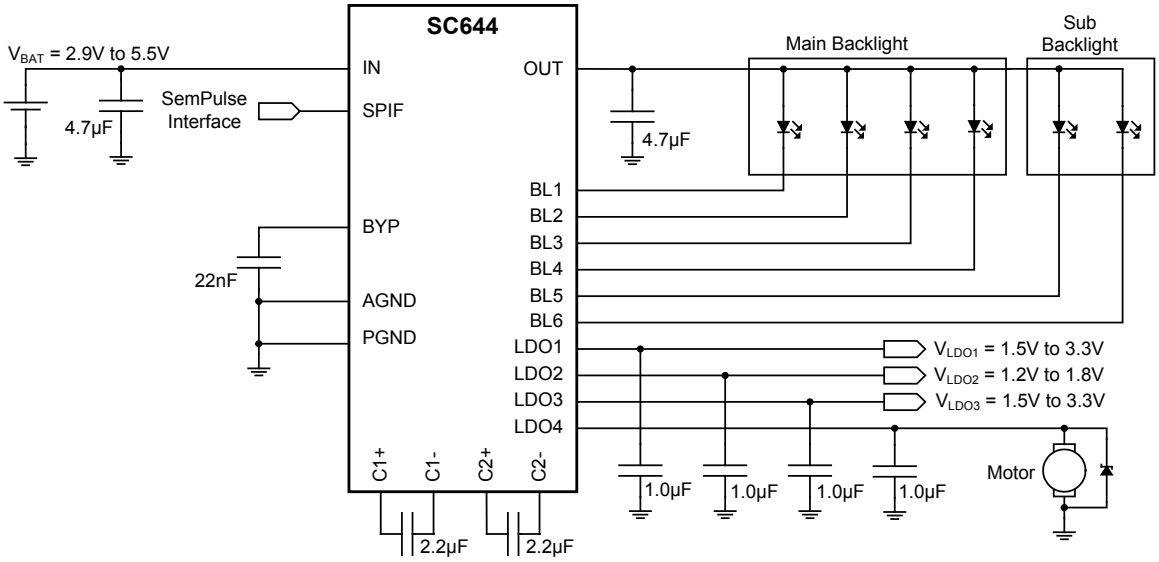
The SC644 is a high efficiency charge pump LED driver using Semtech's proprietary charge pump technology. Performance is optimized for use in single cell Li-ion battery applications.

Display backlighting is provided through six matched current sinks with integrated fade-in and fade-out controls. The LEDs can be driven as a single set or as two different sets (for main and sub displays) with independent controls. Four low noise, low dropout (LDO) regulators are provided to supply power for camera module I/O and other peripheral circuits.

The SC644 uses the proprietary SemPulse® single wire interface. This interface controls all functions of the device, including backlight currents and LDO voltage outputs. The single wire interface minimizes microcontroller and interface pin counts.

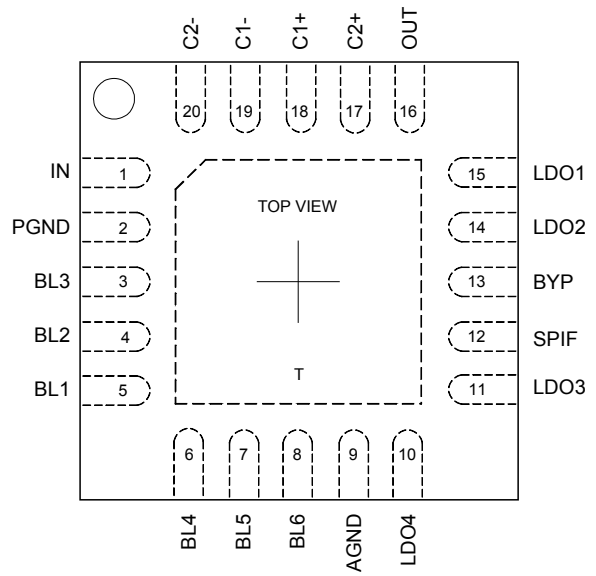
The SC644 enters sleep mode when all the LED drivers are disabled. In this mode, the quiescent current is reduced while the device continues to monitor the SemPulse interface. Any combination of LDOs may be enabled when in sleep mode.

Typical Application Circuit



US Patents: 6,504,422; 6,794,926

Pin Configuration



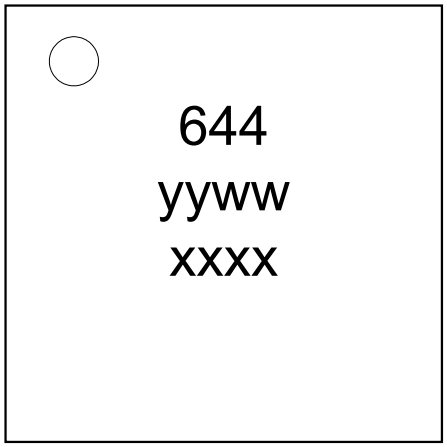
MLPQ-UT-20; 3x3, 20 LEAD
θ_{JA} = 35°C/W

Ordering Information

Device	Package
SC644ULTRT[1][2]	MLPQ-UT-20 3×3
SC644EVB	Evaluation Board

Notes:
(1) Available in tape and reel only. A reel contains 3,000 devices.
(2) Lead-free packaging only. Device is WEEE and RoHS compliant, and halogen free.

Marking Information



yyww = Date Code
xxxx = Semtech Lot No.

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Absolute Maximum Ratings

IN, OUT (V) ..... -0.3 to +6.0
C1+, C2+ (V) ..... -0.3 to (V_{OUT} + 0.3)
Pin Voltage — All Other Pins (V) ..... -0.3 to (V_{IN} + 0.3)
OUT, LDOn[1] Short Circuit Duration ..... Continuous
ESD Protection Level[2] (kV) 2

Recommended Operating Conditions

Ambient Temperature Range (°C) ..... $-40 \le T_A \le +85$
Input Voltage (V) ..... $2.9 \le V_{IN} \le 5.5$
Output Voltage (V) ..... $2.5 \le V_{OUT} \le 5.25$
Voltage difference between any two LEDs (V) ... $\Delta V_F \le 1.0$

Thermal Information

Thermal Resistance, Junction to Ambient[3] (°C/W) 35
Maximum Junction Temperature (°C) ..... +150
Storage Temperature Range (°C) ..... -65 to +150
Peak IR Reflow Temperature (10s to 30s) (°C) ..... +260

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES:
(1) subscript n = 1, 2, 3, and 4.
(2) Tested according to JEDEC standard JESD22-A114-B.
(3) Calculated from package in still air, mounted to 3 x 4.5 (in), 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

Electrical Characteristics

Unless otherwise noted, T_A = +25°C for Typ, -40°C to +85°C for Min and Max, $T_{J(MAX)}$ = 125°C, V_{IN} = 3.7V, C_1= C_2 = 2.2µF, C_{IN} = C_{OUT} = 4.7µF, (ESR = 0.03Ω)[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Specifications						
Input Supply Voltage	V_{IN}		2.9		5.5	V
Shutdown Current	$I_{Q(OFF)}$	Shutdown, V_{IN} = 4.2V		0.1	2.0	µA
Total Quiescent Current	I_Q	Sleep (all LDOs off), SPIF = V_{IN}[2]		90	135	µA
		Sleep (all LDOs on), SPIF = V_{IN}[2]		300	450	
		1x mode, I_{OUT} = 3.0 mA, I_{BLn}[3] = 0.5mA, 6 LEDs on		2.6		mA
		1x mode, I_{OUT} = 150mA, I_{BLn} = 25mA, 6 LEDs on		4.8		
		1.5x or 2x mode, I_{OUT} = 150mA, I_{BLn} = 25mA, 6 LEDs on		5.6		
Charge Pump Electrical Specifications						
Maximum Total Output Current	$I_{OUT(MAX)}$	Sum of all active LED currents, $V_{OUT} \le 4.2V$	150			mA
Backlight Current Setting Range	I_{BL}	Nominal setting for BL1 – BL6	0		25	mA
Backlight Current Accuracy	I_{BL_ACC}	I_{BLn} = 12mA	-8	±1.5	8	%
Backlight Current Matching[4]	I_{BL-BL}	I_{BLn} = 12mA	-3.5	±0.5	+3.5	%
1x Mode to 1.5x Mode Falling Transition Voltage	$V_{TRANS1x}$	I_{OUT} = 50mA, I_{BLn} = 10mA, V_{OUT} = 3.2V		3.22		V
1.5x Mode to 1x Mode Hysteresis	V_{HYST1x}	I_{OUT} = 50mA, I_{BLn} = 10mA, V_{OUT} = 3.2V		250		mV

Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Charge Pump Electrical Specifications (Cont.)						
1.5x Mode to 2x Mode Falling Transition Voltage	$V_{TRANS1.5x}$	I_{OUT} = 50mA, I_{BLn} = 10mA, V_{OUT} = 4.2V[5]		2.91		V
2x Mode to 1.5x Mode Hysteresis	$V_{HYST1.5x}$	I_{OUT} = 50mA, I_{BLn} = 10mA, V_{OUT} = 4.2V[5]		520		mV
Current Sink Off-State Leakage Current	$I_{BL/FL(OFF)}$	$V_{IN} = V_{BLn}$ = 4.2V		0.1	1	µA
Pump Frequency	f_{PUMP}	V_{IN} = 3.2V		250		kHz
LDO Electrical Specifications						
LDO1, LDO3, and LDO4 Voltage Setting Range	V_{LDOm}[6]	Range of nominal settings	1.5		3.3	V
LDO2 Voltage Setting Range	V_{LDO2}	Range of nominal settings	1.2		1.8	V
Output Voltage Accuracy	ΔV_{LDO}	I_{LDO} = 1mA, T_A = 25°C, 2.9V ≤ V_{IN} ≤ 4.2V	-3	±1.0	+3	%
		I_{LDO} = 1mA to 100mA, 2.9V ≤ V_{IN} ≤ 4.2V	-3.5		+3.5	%
Dropout Voltage[6][7]	V_{Dm}	I_{LDOm} = 150mA, $V_{IN} = V_{LDOm} + V_{Dm}$		150	200	mV
Current Limit	I_{LIM}		200			mA
Line Regulation	ΔV_{LINE}	I_{LDOm} = 1mA, V_{IN} = 2.9V to 4.2V, V_{LDOm} = 2.8V		2.1	7.2	mV
		I_{LDO2} = 1mA, V_{IN} = 2.9V to 4.2V, V_{LDO2} = 1.8V		1.3	4.8	
Load Regulation	ΔV_{LOAD}	V_{LDOm} = 3.3V, I_{LDOm} = 1mA to 100mA			25	mV
		V_{LDO2} = 1.8V, I_{LDO2} = 1mA to 100mA			20	
Power Supply Rejection Ratio	$PSRR_m$	1.5V < V_{LDOm} < 3.0V, f < 1kHz, C_{BYP} = 22nF, I_{LDOm} = 50mA, with 0.5V_{P-P} supply ripple		50		dB
	$PSRR_2$	1.2V < V_{LDO2} < 1.8V, f < 1kHz, C_{BYP} = 22nF, I_{LDO2} = 50mA, with 0.5V_{P-P} supply ripple		60		
Output Voltage Noise	e_{n-LDOm}	10Hz < f < 100kHz, C_{BYP} = 22nF, C_{LDOm} = 1µF, I_{LDOm} = 50 mA, 1.5V < V_{LDOm} < 3.0V		75		μV_{RMS}
	e_{n-LDO2}	10Hz < f < 100kHz, C_{BYP} = 22nF, C_{LDO2} = 1µF, I_{LDO2} = 50 mA, 1.2V < V_{LDO2} < 1.8V		50		
Minimum LDO Capacitor [8]	$C_{LDO(MIN)}$	Nominal value for C_{LDOn}	1			µF

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Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Digital I/O Electrical Specifications (SPIF)						
Input High Threshold (9)	V_{IH}	V_{IN} = 5.5V	1.6			V
Input Low Threshold (9)	V_{IL}	V_{IN} = 2.9V			0.4	V
Input High Current	I_{IH}	V_{IN} = 5.5V	-1		+1	µA
Input Low Current	I_{IL}	V_{IN} = 5.5V	-1		+1	µA
SemPulse Electrical Specifications (SPIF)						
SemPulse Start-up Time(10)	t_{SU}		1			ms
Bit Pulse Duration (9)	t_{HI}		0.75		250	µs
Duration Between Bits (9)	t_{LO}		0.75		250	µs
Hold Time - Address (9)	t_{HOLDA}	SPIF is held high	500		5000	µs
Hold Time - Data (9)	t_{HOLDD}	SPIF is held high	500			µs
Bus Reset Time (9)	t_{BR}	SPIF is held high	10			ms
Shutdown Time(11)	t_{SD}	SPIF is pulled low	10			ms
Fault Protection						
Output Short Circuit Current Limit	$I_{OUT(SC)}$	OUT pin shorted to GND		300		mA
Over-Temperature	T_{OTP}	Rising threshold		165		°C
	T_{HYS}	Hysteresis		30		°C
Charge Pump Over-Voltage Protection	V_{OVP}	OUT pin open circuit, $V_{OUT} = V_{OVP}$		5.7	6.0	V
Under Voltage Lockout	$V_{UVLO-OFF}$	Increasing V_{IN}		2.7		V
	$V_{UVLO-HYS}$	Hysteresis		800		mV

Notes:

(1) Capacitors are MLCC of X5R type. Production tested with higher value capacitors than the application requires.

(2) SPIF is high for more than 10ms

(3) Subscript for all backlights (BLn), n = 1, 2, 3, 4, 5, and 6. Subscripting for all LDOs (LDOn), n = 1, 2, 3, 4.

(4) Current matching is defined as $\pm [I_{BL(MAX)} - I_{BL(MIN)}] / [I_{BL(MAX)} + I_{BL(MIN)}]$.

(5) Test voltage is V_{OUT} = 4.2V — a relatively extreme LED voltage — to force a transition during test. Typically V_{OUT} = 3.2V for white LEDs.

(6) Subscript m = 1, 3, and 4 and applies only to LDO1, LDO3, and LDO4.

(7) Dropout is defined as (V_{IN}-V_{LDOm}) when V_{LDOm} drops 100mV from nominal. Dropout does not apply to LDO2 since it has a maximum output voltage of 1.8V.

(8) X5R or better "temperature stable" MLCC capacitor.

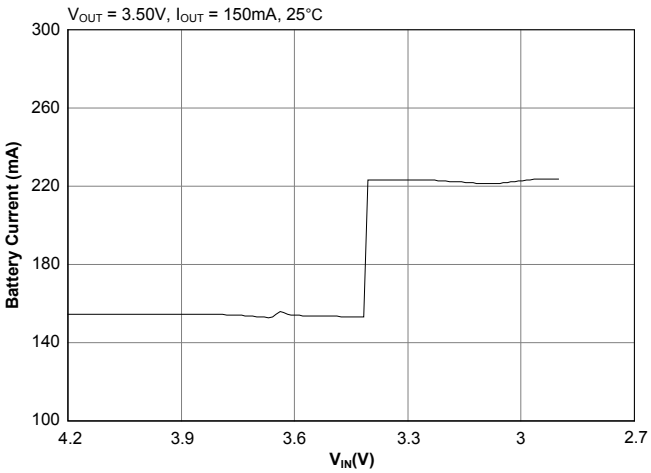
(9) The source driver used to provide the SemPulse output must meet these limits.

(10) The SemPulse start-up time is the minimum time that the SPIF pin must be held high to enable the part before commencing communication.

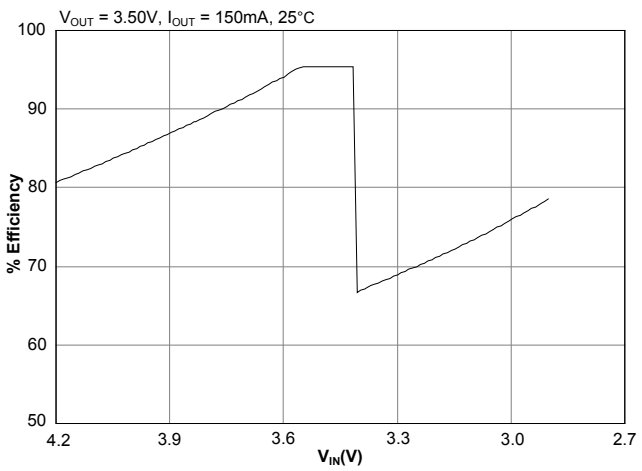
(11) The SemPulse shutdown time is the minimum time that the SPIF pin must be pulled low to shut the part down.

Typical Characteristics

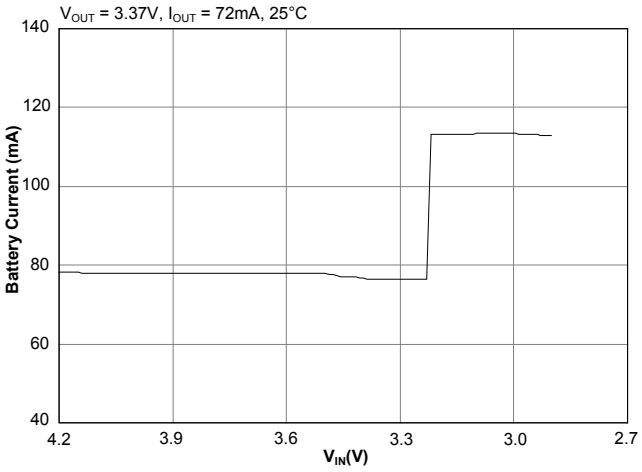
Battery Current (6 LEDs) — 25mA Each



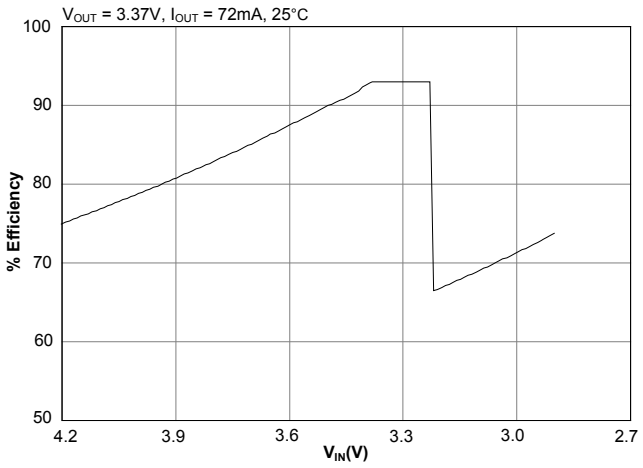
Backlight Efficiency (6 LEDs) — 25mA Each



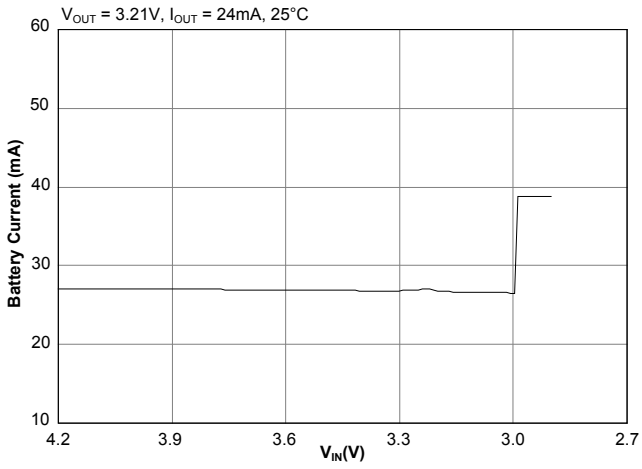
Battery Current (6 LEDs) — 12mA Each



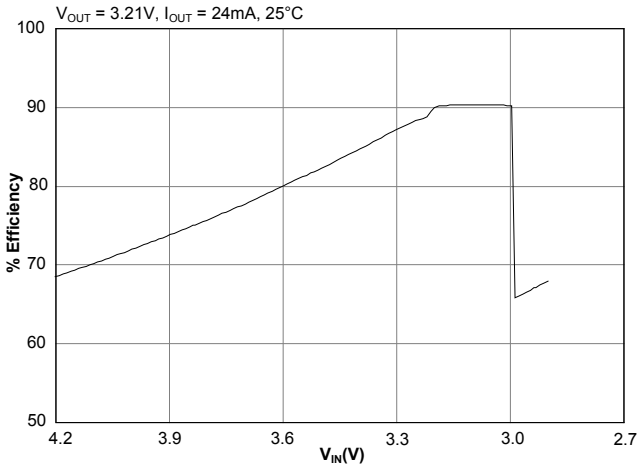
Backlight Efficiency (6 LEDs) — 12mA Each



Battery Current (6 LEDs) — 4.0mA Each

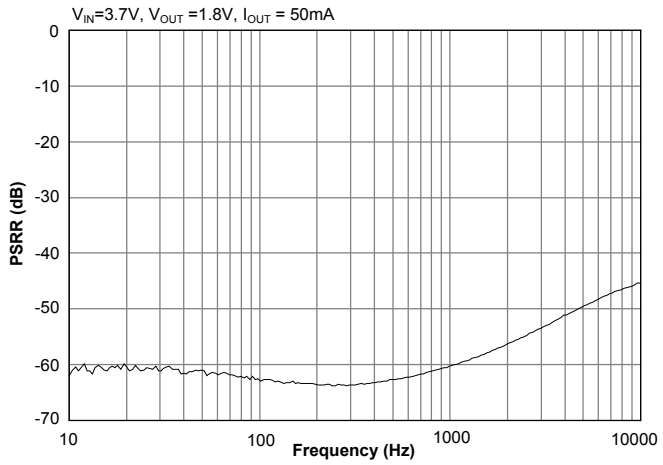


Backlight Efficiency (6 LEDs) — 4.0mA Each

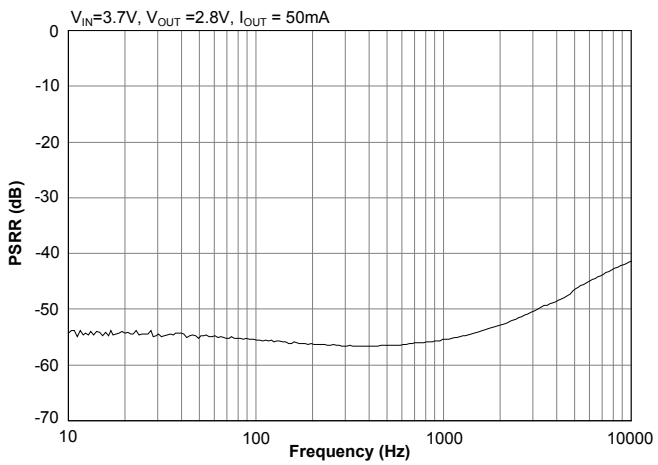


Typical Characteristics (continued)

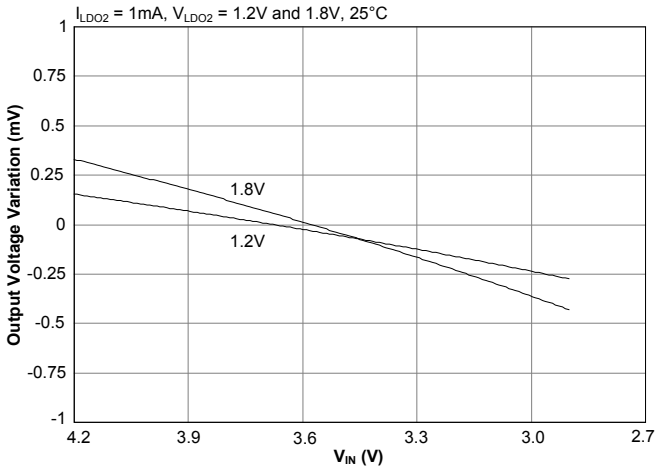
PSRR vs. Frequency — 1.8V



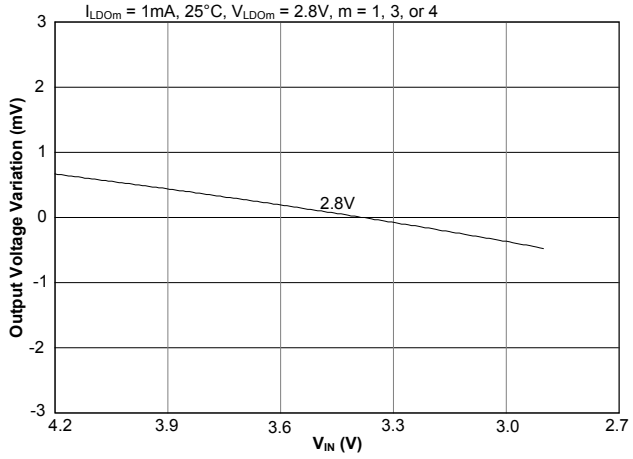
PSRR vs. Frequency — 2.8V



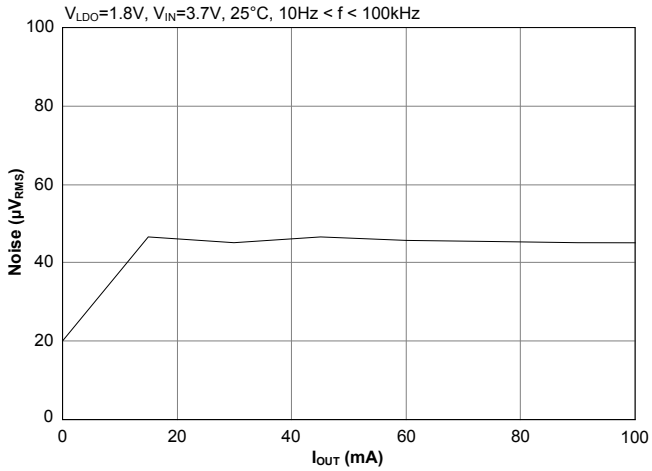
Line Regulation (LDO2)



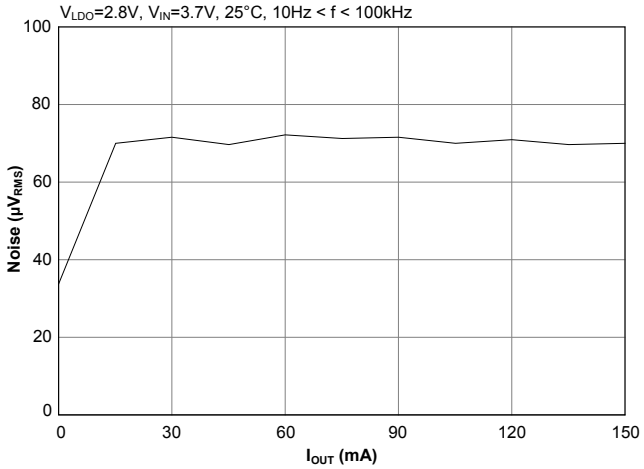
Line Regulation (LDOm)



LDO Noise vs. Load Current — 1.8V

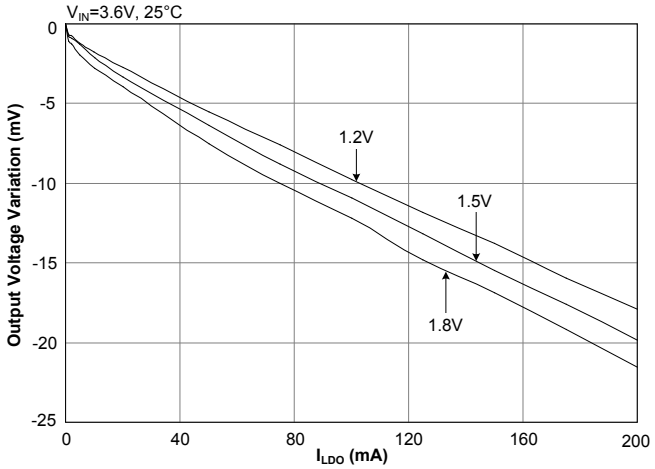


LDO Noise vs. Load Current — 2.8V

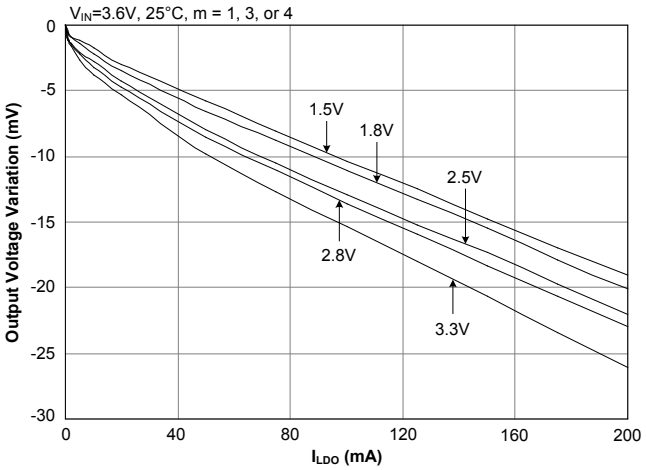


Typical Characteristics (continued)

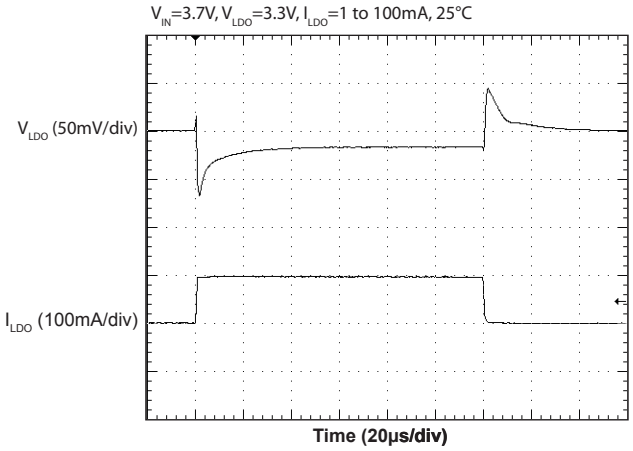
Load Regulation (LDO2)



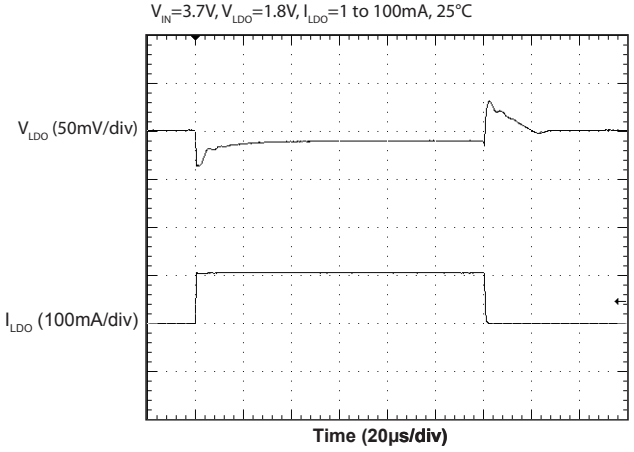
Load Regulation (LDOm)



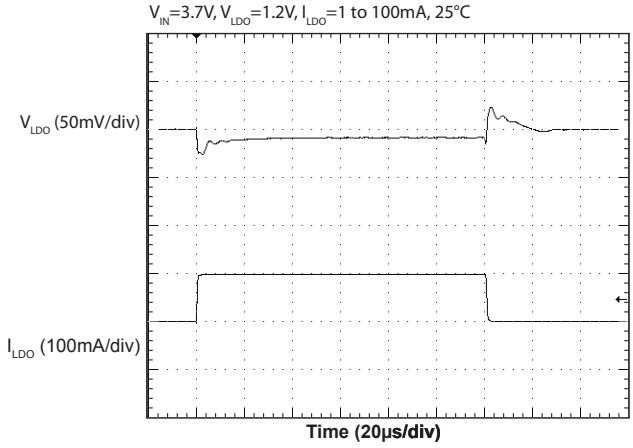
LDO Load Transient Response (3.3V)



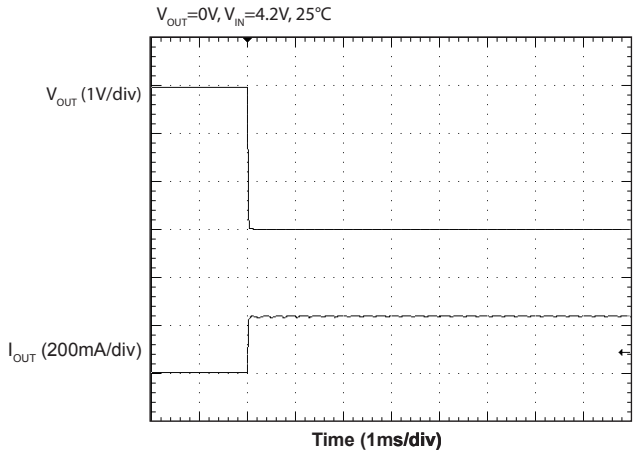
LDO Load Transient Response (1.8V)



LDO Load Transient Response (1.2V)

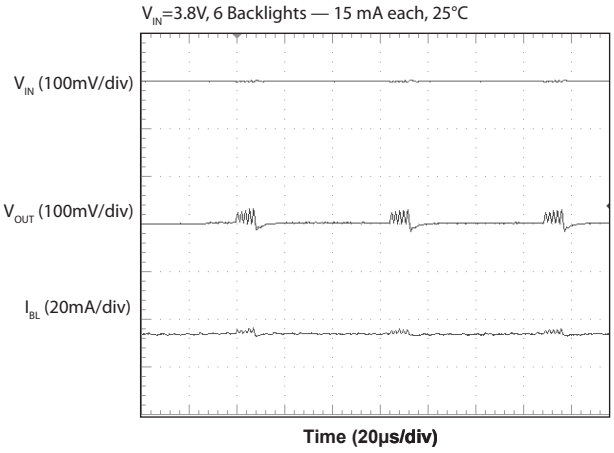


Output Short Circuit Current Limit

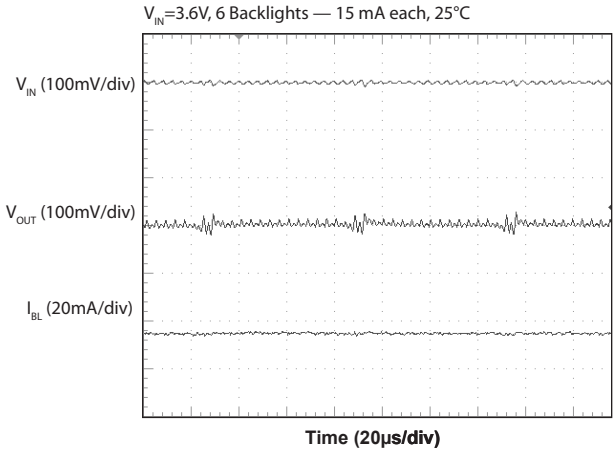


Typical Characteristics (continued)

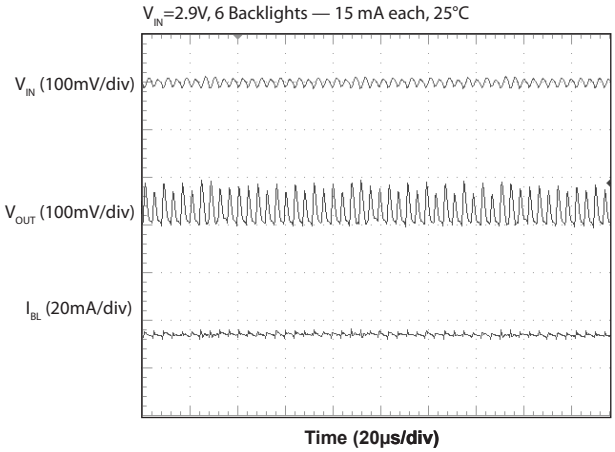
Ripple — 1X Mode



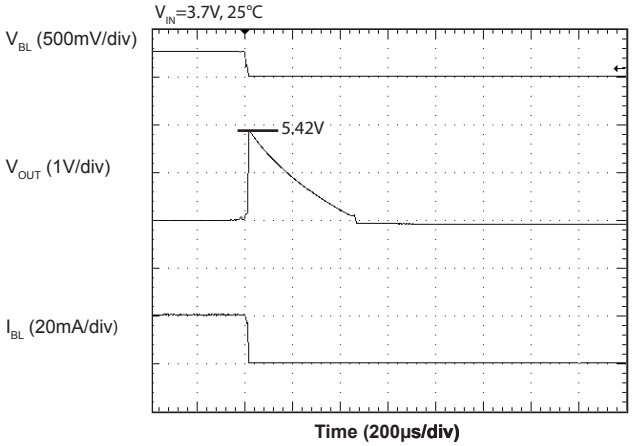
Ripple — 1.5X Mode



Ripple — 2X Mode



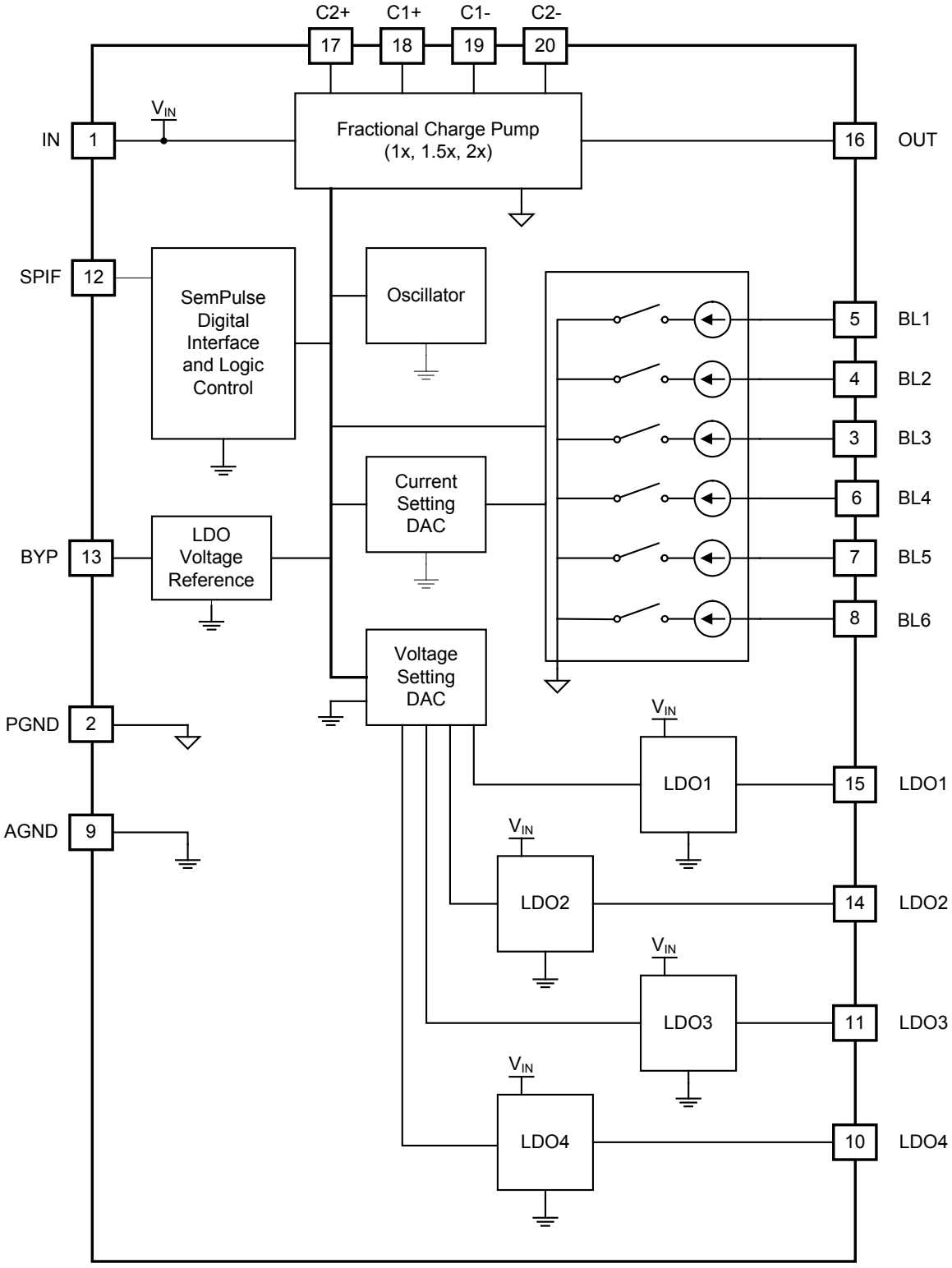
Output Open Circuit Protection



Pin Descriptions

Pin #	Pin Name	Pin Function
1	IN	Battery voltage input
2	PGND	Ground pin for high current charge pump
3	BL3	Current sink output for backlight LED 3 — leave this pin open if unused
4	BL2	Current sink output for backlight LED 2 — leave this pin open if unused
5	BL1	Current sink output for backlight LED 1 — leave this pin open if unused
6	BL4	Current sink output for backlight LED 4 — leave this pin open if unused
7	BL5	Current sink output for backlight LED 5 — leave this pin open if unused
8	BL6	Current sink output for backlight LED 6 — leave this pin open if unused
9	AGND	Analog ground pin — connect to ground and separate from PGND current
10	LDO4	Output of LDO4
11	LDO3	Output of LDO3
12	SPIF	SemPulse single wire interface pin — used to enable/disable the device and to configure all registers (refer to Register Map and SemPulse Interface sections)
13	BYP	Bypass pin for LDO reference — connect a 22nF ceramic capacitor to AGND
14	LDO2	Output of LDO2
15	LDO1	Output of LDO1
16	OUT	Charge pump output — all LED anode pins should be connected to this pin
17	C2+	Positive connection to bucket capacitor 2
18	C1+	Positive connection to bucket capacitor 1
19	C1-	Negative connection to bucket capacitor 1
20	C2-	Negative connection to bucket capacitor 2
T	THERMAL PAD	Thermal pad for heatsinking purposes — connect to ground plane using multiple vias — not connected internally

Block Diagram



Applications Information

General Description

This design is optimized for handheld applications supplied from a single cell Li-Ion and includes the following key features:

- A high efficiency fractional charge pump that supplies power to all LEDs
- Six matched current sinks that control LED backlighting current, with 0mA to 25mA per LED.
- Four adjustable LDOs. LDO1 , LDO3, and LDO4 are adjustable with 15 settings from 1.5V to 3.3V. LDO2 is adjustable with 7 settings from 1.2V to 1.8V.

High Current Fractional Charge Pump

The backlight outputs are supported by a high efficiency, high current fractional charge pump output. The charge pump multiplies the input voltage by 1, 1.5 or 2 times. The charge pump switches at a fixed frequency of 250kHz in 1.5x and 2x modes and is disabled in 1x mode to save power and improve efficiency.

The mode selection circuit automatically selects the mode as 1x, 1.5x, or 2x based on circuit conditions such as LED voltage, input voltage, and load current. The 1x mode is the most efficient of the three modes, followed by 1.5x and 2x modes. Circuit conditions such as low input voltage, high output current, or high LED voltage place a higher demand on the charge pump output. A higher numerical mode (1.5x or 2x) may be needed momentarily to maintain regulation at the OUT pin during intervals of high demand. The charge pump responds to momentary high demands, setting the charge pump to the optimum mode to deliver the output voltage and load current while optimizing efficiency. Hysteresis is provided to prevent mode toggling.

The charge pump requires two bucket capacitors for proper operation. One capacitor must be connected between the C1+ and C1- pins and the other must be connected between the C2+ and C2- pins as shown in the typical application circuit diagram. These capacitors should be equal in value, with a nominal capacitance of 2.2µF to support the charge pump current requirements. The device also requires a 4.7µF capacitor on the IN pin and a 4.7µF capacitor on the OUT pin to minimize noise and support the output drive requirements. Capacitors with X7R or X5R ceramic dielectric are strongly recommended for their low ESR and superior temperature and voltage characteristics. Y5V capacitors should not be used as their temperature coefficients make them unsuitable for this application.

LED Backlight Current Sinks

The backlight current is set via the SemPulse interface. The current is regulated to one of 29 values between 0mA and 25mA. The step size varies depending upon the current setting. Between 0mA and 5mA, the step size is 0.5mA. The step size increases to 1mA for settings between 5mA and 21mA. Steps are 2mA between 21mA and 25mA. The variation in step size allows finer adjustment for dimming functions in the low current setting range and coarse adjustment at higher current settings where small current changes are not visibly noticeable in LED brightness. A zero setting is also included to allow the current sink to be disabled by writing to either the enable bit or the current setting register for maximum flexibility.

All backlight current sinks have matched currents, even when there is variation in the forward voltages (ΔV_F) of the LEDs. A minimum ΔV_F of 1.2V is supported when the input voltage (V_{IN}) is at 3.0V. Higher ΔV_F LED mis-match is supported when V_{IN} is higher than 3.0V. All current sink outputs are compared and the lowest output is used for setting the voltage regulation at the OUT pin. This is done to ensure that sufficient bias exists for all LEDs.

The backlight LEDs default to the off state upon power-up. For backlight applications using fewer than six LEDs, any unused output must be left open and the unused LED must remain disabled. When writing to the backlight enable register, a zero (0) must be written to the corresponding bit of any unused output.

Backlight Quiescent Current

The quiescent current required to operate all five backlights is reduced when backlight current is set to 4.0mA or less. This feature results in higher efficiency under light-load conditions. Further reduction in quiescent current will result from using fewer than six LEDs.

Applications Information (continued)

Main and Sub Backlight Bank Configuration

The six LED backlight drivers can be configured as a single bank or as two independent banks — one dedicated for a main display and the other for a sub display. This feature allows the device to drive two sets of LEDs with different settings so different current and fade settings can be used.

The Register Map contains two separate control registers for main and sub currents. Register 01h contains the current setting code for the main bank, and register 02h contains the setting code for the sub bank. There are also three bits in register 0Ah that control which drivers are assigned to each display. The default setting assigns all six LED drivers to the main display control register. In this scenario, the current control settings for each LED driver come from register 01h. Other settings are available that allow the groupings to be defined so that any number from 1 to 6 drivers can be grouped as the main display backlight drivers, with the remaining drivers assigned to the sub display backlight by default. See Table 8 of the Register Map section for more details.

Backlight Fade-in and Fade-out Function

Register 09h contains bits that control the fade state of each display (main and sub). When enabled, the fade function causes the backlight settings to step from their current state to the next programmed state as soon as the new state is stored in its register. For example, if the backlight is set at 25mA and the next setting is the off state, the backlight will step from 25mA down to 0mA using all 29 settings at the fade rate specified by the bits in register 09h. The same is true when turning on or increasing the backlight current — the backlight current will step from the present level to the new level at the step rate defined in register 09h. This process applies for both the main and the sub displays. The state diagram in Figure 1 describes all possible conditions for a fade operation. More details can be found in the Register Map section.

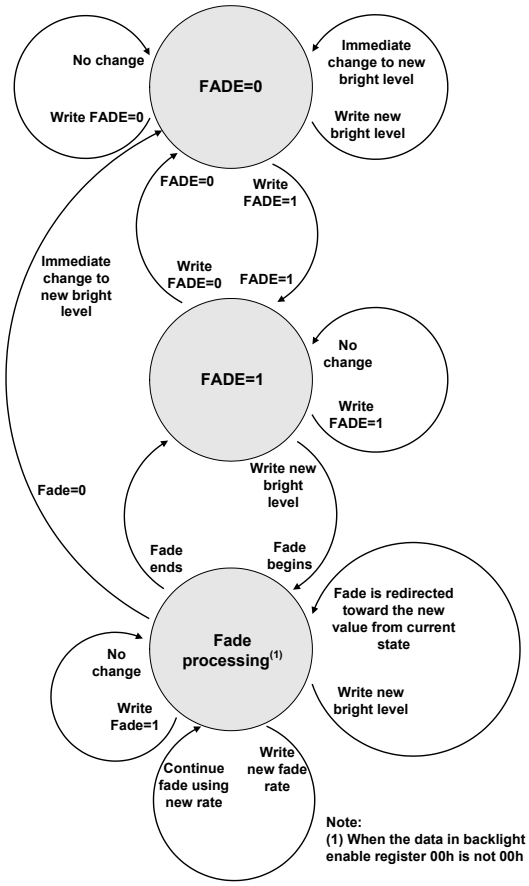


Figure 1 — State Diagram for Fade Function

Fade-In from Off State

When the initial state of the main or sub backlight current register is 00h (the data value for 0mA), fading to an on state is accomplished by following the steps listed in Table 1. Following these steps explicitly will ensure that the fade-in operation will proceed with no interruption at the rate specified in the Main/Sub Backlight Fade register (09h). This procedure must be followed regardless of which backlight grouping configuration is being used. Note that it is only necessary to set the BLEN bits for the main or sub display that is required to fade.

Applications Information (continued)

Table 1 — Fade-In from Off State

Command Sequence	Action	Data
1. Disable fade for the bank	Write to register 09h	Binary value xx0xxx, xxxxx0, or xx0xx0
2. Set Main and/or Sub backlights to 0.5mA	Write to register 01h and or 02h(1)	04h
3. Enable fade for the bank	Write to register 09h	Binary value xx1xx0 , xx1xx1, or xx0xx1
4. Set BLEN bits	Write to register 00h	Any value from 01h through 3Fh
5. Set new value of backlight current for the bank	Write to register 01h and/or 02h	Any value from 05h through 1Fh

Notes:
(1) Write only to the banks which will fade

Fade-Out from any On State to Off State

Fading the backlight LEDs from any active state to the off state follows a simple procedure. The sequence of commands for this action is shown in Table 2. Following these steps explicitly will ensure that the fade-out operation will proceed with no interruption at the rate specified in the Main/Sub Backlight Fade register (09h). This procedure must be followed regardless of the backlight grouping configuration.

Table 2 — Fade-Out from any On State to Off State

Command Sequence	Action	Data
1. Enable fade	Write to register 09h	Any value from 01h through 3Fh
2. Set Main and/or Sub backlights to 0mA	Write to register 01h and/or 02h	00h

Fading Between Different On States

Fading from one backlight level to another (up or down) also follows a simple procedure. The sequence of commands for this action is shown in Table 3. Following these steps explicitly will ensure that the fade-in/fade-out operation will proceed with no interruption at the rate specified in the Main/Sub Backlight Fade register (09h). This procedure must be followed regardless of the backlight grouping configuration.

Table 3 — Fading between Different On States

Command Sequence	Action	Data
1. Enable fade	Write to register 09h	Any value from 01h through 3Fh
2. Set new value of backlight current	Write to register 01h and/or 02h	Any value from 05h through 1Fh

Additional Information

For more details about the Fade-in/Fade-out function, refer to the *SC644 Backlight Driver Software User's Guide* and *SemPulse Interface Specification* document and to the associated software drivers available for this device (contact your sales office for more details).

Programmable LDO Outputs

Four low dropout (LDO) regulators are included to supply power to peripheral circuits. Each LDO output voltage setting has ±3.5% accuracy over the operating temperature range. Output current greater than specification is possible at somewhat reduced accuracy (refer to the typical characteristic section of this datasheet for load regulation examples). LDO1, LDO3, and LDO4 have identical specifications, with a programmable output ranging from 1.5V to 3.3V. LDO2 is specified to operate with programmable output ranging from 1.2V to 1.8V. LDO2 also has lower noise specifications so that it can be used with noise sensitive circuits.

Shutdown Mode

The device is disabled when the SPIF pin is held low for the shutdown time specified in the electrical characteristics section. All registers are reset to default condition at shutdown. Typical current consumption is this mode is 0.1µA

Sleep Mode

When all backlights are off the charge pump is disabled, and sleep mode is activated. This is a reduced current mode that helps minimize overall current consumption. In sleep mode, the SemPulse interface continues to monitor its input for commands from the host. Typical current consumption in this mode is 90µA.

Applications Information (continued)

Protection Features

The SC644 provides several protection features to safeguard the device from catastrophic failures. These features include:

- Output Open Circuit Protection
- Over-Temperature Protection
- Charge Pump Output Current Limit
- LDO Current Limit
- LED Float Detection

Output Open Circuit Protection

Over-Voltage Protection (OVP) at the OUT pin prevents the charge pump from producing an excessively high output voltage. In the event of an open circuit between the OUT pin and all current sinks (no loads connected), the charge pump runs in open loop and the voltage rises up to the OVP limit. OVP operation is hysteretic, meaning the charge pump will momentarily turn off until V_{OUT} is sufficiently reduced. The maximum OVP threshold is 6.0V, allowing the use of a ceramic output capacitor rated at 6.3V with no concern of over-voltage damage. Typical OVP voltage is 5.7V.

Over-Temperature Protection

The Over-Temperature (OT) protection circuit prevents the device from overheating and experiencing a catastrophic failure. When the junction temperature exceeds 165°C, the device goes into thermal shutdown with all outputs disabled until the junction temperature is reduced. All register information is retained during thermal shutdown. Hysteresis of 30°C is provided to ensure that the device cools sufficiently before re-enabling.

Charge Pump Output Current Limit

The device limits the charge pump current at the OUT pin. When OUT is shorted to ground, the output current will typically equal 300mA. The output current is also limited to 300mA when over loaded resistively.

LDO Current Limit

The device limits the current at all LDO output pins. The minimum limit is 200mA, so load current of greater than the rated current can be used (with degraded accuracy) without tripping the current limit.

LED Float Detection

Float detect is a fault detection feature of the LED backlight outputs. If an output is programmed to be enabled and an open circuit fault occurs at any backlight output, that output will be disabled to prevent a sustained output OVP condition from occurring due to the resulting open loop. Float detect ensures device protection but does not ensure optimum performance. Unused LED outputs must be disabled to prevent an open circuit fault from occurring.

Thermal Management

The device has the potential for peak power dissipation equal to 2.75W when all outputs are simultaneously operating at maximum rated current and powered by a fully charged Li-Ion cell equal to 4.2V. A calculation of the maximum power dissipation of the device should be done to identify if power management measures are needed to prevent overheating. The MLP package is capable of dissipating 1.85W when proper layout techniques are used.

Applications Information (continued)

PCB Layout Considerations

The layout diagram in Figure 2 illustrates a proper two-layer PCB layout for the SC644 and supporting components. Following fundamental layout rules is critical for achieving the performance specified in the Electrical Characteristics table. The following guidelines are recommended when developing a PCB layout:

- Place all bypass and decoupling capacitors — C1, C2, CIN, COUT, CLDO1, CLDO2, CLDO3, CLDO4, and CBYP as close to the device as possible.
- All charge pump current passes through IN, OUT, and the bucket capacitor connection pins. Ensure that all connections to these pins make use of wide traces so that the resistive drop on each connection is minimized.
- The thermal pad should be connected to the ground plane using multiple vias to ensure proper thermal connection for optimal heat transfer.
- The following capacitors — CLDO1, CLDO2, CLDO3, CLDO4, and CBYP should be grounded together. Connect these capacitors to the ground plane at one point near the AGND pin as shown in Figure 2.

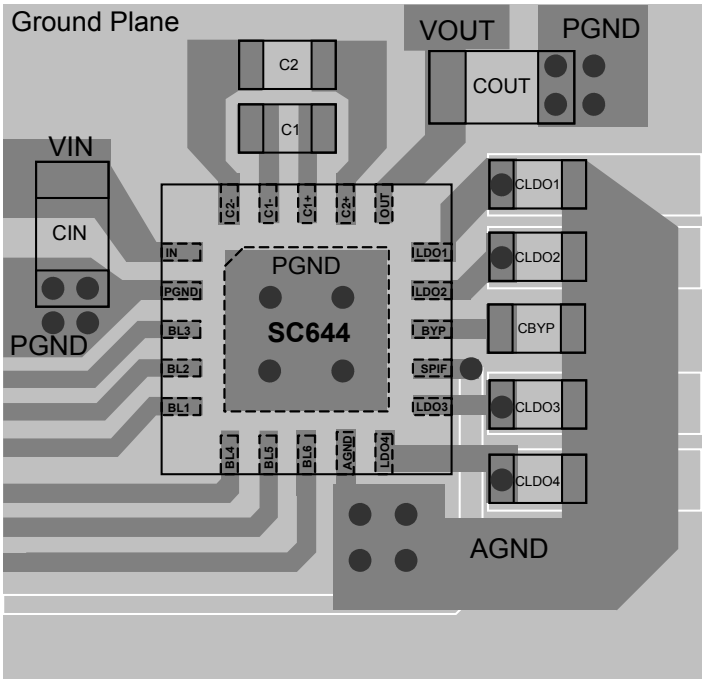


Figure 2 — Recommended PCB Layout

- Figure 3 shows the pads that should be connected to the ground plane with multiple vias. Make all ground connections to a solid ground plane as shown in Figure 4.
- If a ground layer is not feasible, the following groupings should be connected:
  - PGND — CIN, COUT
  - AGND — Ground Pad, CLDO1, CLDO2, CLDO3, CLDO4, CBYP
- If no ground plane is available, PGND and AGND should be routed back to the negative battery terminal, separately, using thick traces. Joining the two ground returns at the terminal prevents large pulsed return currents from mixing with the low-noise return currents of the LDOs.
- All LDO output traces should be made as wide as possible to minimize resistive losses.

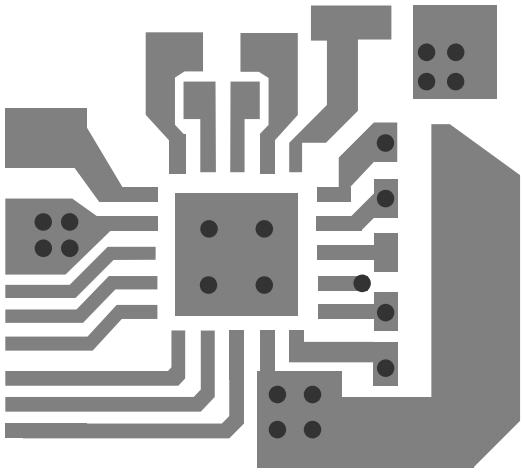


Figure 3 — Layer 1

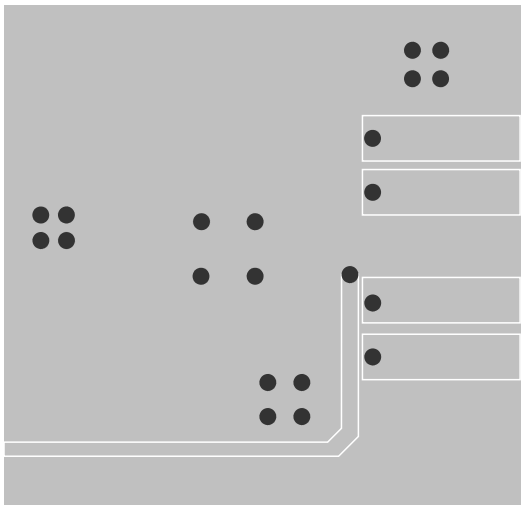


Figure 4 — Layer 2

SEMTECH

SemPulse® Interface

Introduction

SemPulse is a write-only single wire interface. It provides access to up to 32 registers that control device functionality. Two sets of pulse trains are transmitted to generate a complete SemPulse command. The first pulse set is used to set the desired address. After the bus is held high for the address hold period, the next pulse set is used to write the data value. After the data pulses are transmitted, the bus is held high again for the data hold period to signify the data write is complete. At this point the device latches the data into the address that was selected by the first set of pulses. See the SemPulse Timing Diagrams for descriptions of all timing parameters.

Chip Enable/Disable

The device is enabled when the SemPulse interface pin (SPIF) is pulled high for greater than t_{SU}. If the SPIF pin is pulled low again for more than t_{SD}, the device will be disabled.

Address Writes

The first set of pulses can range between 0 and 31 (or 1 to 32 rising edges) to set the desired address. After the pulses are transmitted, the SPIF pin must be held high for t_{HOLDA} to signal to the slave device that the address write is finished. If the pulse count is between 0 and 31 and the line is held high for t_{HOLDA}, the address is latched as the destination for the data word. If the SPIF pin is not held high for t_{HOLDA}, the slave device will continue to count pulses. If the total exceeds 31 pulses, the write will be ignored and the bus will reset after the next valid hold time is detected. Note that if t_{HOLDA} exceeds its maximum specification, the bus will reset. This means that the communication is ignored and the bus resumes monitoring the pin, expecting the next pulse set to be an address.

Data Writes

After the bus has been held high for the minimum address hold period, the next set of pulses are used to write the data value. The total number of pulses can range from 0 to 63 (or 1 to 64 rising edges) since there are a total of 6 register bits per register. Just like with the address write, the data write is only accepted if the bus is held high for t_{HOLDD} when the pulse train is completed. If the proper hold time is not received, the interface will keep counting pulses until the hold time is detected. If the total exceeds 63 pulses, the write will be ignored and the bus will reset after the next valid hold time is detected. After the bus has been held high for t_{HOLDD}, the bus will expect the next pulse set to be an address write. Note that this is the same effect as the bus reset that occurs when t_{HOLDA} exceeds its maximum specification. For this reason, there is no maximum limit on t_{HOLDD} — the bus simply waits for the next valid address to be transmitted.

Multiple Writes

It is important to note that this single-wire interface requires the address to be paired with its corresponding data. If it is desired to write multiple times to the same address, the address must always be re-transmitted prior to the corresponding data. If it is only transmitted one time and followed by multiple data transmissions, every other block of data will be treated like a new address. The result will be invalid data writes to incorrect addresses. Note that multiple writes only need to be separated by the minimum t_{HOLDD} for the slave to interpret them correctly. As long as t_{HOLDA} between the address pulse set and the data pulse set is less than its maximum specification but greater than its minimum, multiple pairs of address and data pulse counts can be made with no detrimental effects.

Standby Mode

Once data transfer is completed, the SPIF line must be returned to the high state for at least 10ms to return to the standby mode. In this mode, the SPIF line remains idle while monitoring for the next command. This mode allows the device to minimize current consumption between commands. Once the device has returned to standby mode, the bus is automatically reset to accept the address pulses as the next data block. This safeguard is intended to reset the bus to a known state (waiting for the beginning of a write sequence) if the delay exceeds the reset threshold.

SemPulse® Interface (continued)

SemPulse Timing Diagrams

The SemPulse single wire interface is used to enable or disable the device and configure all registers (see Figure 5). The timing parameters refer to the digital I/O electrical specifications.

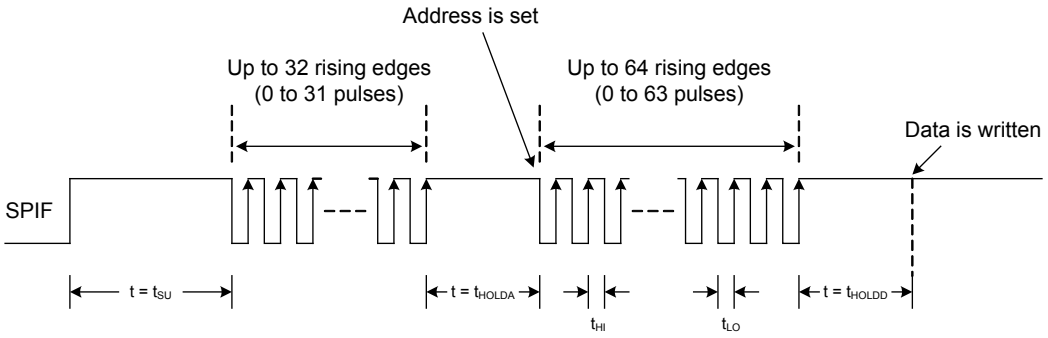


Figure 5 — Uniform Timing Diagram for SemPulse Communication

Timing Example 1

In this example (see Figure 6), the slave chip receives a sequence of pulses to set the address and data, and the pulses experience interrupts that cause the pulse width to be non-uniform. Note that as long as the maximum high and low times are satisfied and the hold times are within specification, the data transfer is completed regardless of the number of interrupts that delay the transmission.

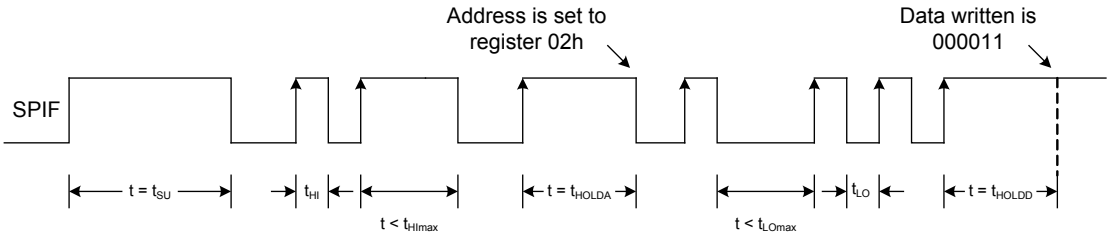


Figure 6 — SemPulse Data Write with Non-Uniform Pulse Widths

Timing Example 2

In this example (see Figure 7), the slave chip receives a sequence of pulses to set the address and data, but an interrupt occurs during a pulse that causes it to exceed the minimum address hold time. The write is meant to be the value 03h in register 05h, but instead it is interpreted as the value 02h written to register 02h. The extended pulse that is delayed by the interrupt triggers a false address detection, causing the next pulse set to be interpreted as the data set. To avoid any problems with timing, make sure that all pulse widths comply with their timing requirements as outlined in this datasheet.

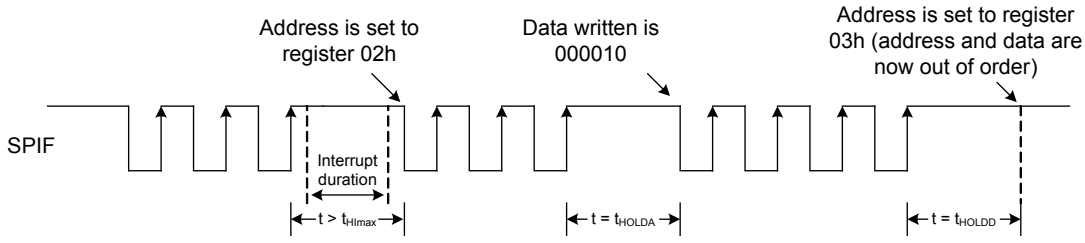


Figure 7 — Faulty SemPulse Data Write Due to Extended Interrupt Duration

Register Map[1]

Address[2]	D5	D4	D3	D2	D1	D0	Reset Value	Description
00h	BL6EN	BL5EN	BL4EN	BL3EN	BL2EN	BL1EN	00h	Backlight Enable
01h	0[3]	MBL4	MBL3	MBL2	MBL1	MBL0	00h	Main Backlight Current
02h	0[3]	SBL4	SBL3	SBL2	SBL1	SBL0	00h	Sub Backlight Current
05h	0[3]	0[3]	LDO1V3	LDO1V2	LDO1V1	LDO1V0	00h	LDO1
06h	0[3]	0[3]	0[3]	LDO2V2	LDO2V1	LDO2V0	00h	LDO2
07h	0[3]	0[3]	LDO3V3	LDO3V2	LDO3V1	LDO3V0	00h	LDO3
08h	0[3]	0[3]	LDO4V3	LDO4V2	LDO4V1	LDO4V0	00h	LDO4
09h	SFADE1	SFADE0	SFADE	MFADE1	MFADE0	MFADE	00h	Main/Sub Backlight Fade
0Ah	0[3]	0[3]	0[3]	MB2	MB1	MB0	00h	Main/Sub Bank Select

Notes:
(1) all registers are write-only
(2) Addresses 03h and 04h are not used
(3) 0 = always write a 0 to these bits

Definition of Registers and Bits

BL Enable Control Register (00h)

This register enables the backlight current sinks.

BL6EN through BL1EN [D5:D0]

These bits are used to enable current sinks. These current sinks will then sink whatever current is set in the corresponding current control register.

Main Backlight Current Control Register (01h)

This register is used to set the currents for the LED drivers designated as main backlight current sinks. Note these current sinks can be disabled using register 00h or by writing the 0mA value into this register.

Bit D5

This bit is unused and is always a zero.

Register Map (continued)

MBL4 through MBL0 [D4:D0]

These bits are used to set the current for the main backlight current sinks. All enabled current sinks will sink the same current as shown in Table 4.

Table 4 — Main Backlight Current Settings

MBL4	MBL3	MBL2	MBL1	MBL0	Backlight Current (mA)
0	0	0	0	0	0
0	0	0	0	1	See note 1
0	0	0	1	0	See note 1
0	0	0	1	1	See note 1
0	0	1	0	0	0.5
0	0	1	0	1	1
0	0	1	1	0	1.5
0	0	1	1	1	2
0	1	0	0	0	2.5
0	1	0	0	1	3
0	1	0	1	0	3.5
0	1	0	1	1	4
0	1	1	0	0	4.5
0	1	1	0	1	5
0	1	1	1	0	6
0	1	1	1	1	7
1	0	0	0	0	8
1	0	0	0	1	9
1	0	0	1	0	10
1	0	0	1	1	11
1	0	1	0	0	12
1	0	1	0	1	13
1	0	1	1	0	14
1	0	1	1	1	15
1	1	0	0	0	16
1	1	0	0	1	17
1	1	0	1	0	18
1	1	0	1	1	19
1	1	1	0	0	20
1	1	1	0	1	21
1	1	1	1	0	23
1	1	1	1	1	25

(1) Reserved for future use.

Sub Backlight Current Control Register (02h)

This register is used to set the currents for the LED drivers designated as sub backlight current sinks. Note these current sinks can be disabled using register 00h or by writing the 0mA value into this register.

Bit D5

This bit is unused and is always a zero.

Register Map (continued)

SBL4 through SBL0 [D4:D0]

These bits are used to set the current for the sub backlight current sinks. All enabled current sinks will sink the same current as shown in Table 5.

Table 5 — Sub Backlight Current Settings

SBL4	SBL3	SBL2	SBL1	SBL0	Backlight Current (mA)
0	0	0	0	0	0
0	0	0	0	1	See note 1
0	0	0	1	0	See note 1
0	0	0	1	1	See note 1
0	0	1	0	0	0.5
0	0	1	0	1	1
0	0	1	1	0	1.5
0	0	1	1	1	2
0	1	0	0	0	2.5
0	1	0	0	1	3
0	1	0	1	0	3.5
0	1	0	1	1	4
0	1	1	0	0	4.5
0	1	1	0	1	5
0	1	1	1	0	6
0	1	1	1	1	7
1	0	0	0	0	8
1	0	0	0	1	9
1	0	0	1	0	10
1	0	0	1	1	11
1	0	1	0	0	12
1	0	1	0	1	13
1	0	1	1	0	14
1	0	1	1	1	15
1	1	0	0	0	16
1	1	0	0	1	17
1	1	0	1	0	18
1	1	0	1	1	19
1	1	1	0	0	20
1	1	1	0	1	21
1	1	1	1	0	23
1	1	1	1	1	25

(1) Reserved for future use.

LDO1 Control Register (05h)

This register is used to enable LDO1 and set its output voltage level.

Bits [D5:D4]

These bits are unused and are always zeroes.

LDO1V3 through LDO1V0 [D3:D0]

These bits set the output voltage of LDO1 as shown in Table 6.

Table 6 — LDO1 Control Codes

LDO1V3	LDO1V2	LDO1V1	LDO1V0	V_{LDO1}
0	0	0	0	OFF
0	0	0	1	3.3V
0	0	1	0	3.2V
0	0	1	1	3.1V
0	1	0	0	3.0V
0	1	0	1	2.9V
0	1	1	0	2.8V
0	1	1	1	2.7V
1	0	0	0	2.6V
1	0	0	1	2.5V
1	0	1	0	2.4V
1	0	1	1	2.2V
1	1	0	0	1.8V
1	1	0	1	1.7V
1	1	1	0	1.6V
1	1	1	1	1.5V

Register Map (continued)

LDO2 Control Register (06h)

This register is used to enable LDO2 and set its output voltage level.

Bits [D5:D3]

These bits are unused and are always zeroes.

LDO2V2 through LDO2V0 [D2:D0]

These bits are used to set the output voltage of LDO2 in accordance with Table 7.

Table 7 — LDO2 Control Codes

LDO2V2	LDO2V1	LDO2V0	V_{LDO2}
0	0	0	OFF
0	0	1	1.8V
0	1	0	1.7V
0	1	1	1.6V
1	0	0	1.5V
1	0	1	1.4V
1	1	0	1.3V
1	1	1	1.2V

LDO3 Control Register (07h)

This register is used to enable LDO3 and set its output voltage level.

Bits [D5:D4]

These bits are unused and are always zeroes.

LDO3V3 through LDO3V0 [D3:D0]

These bits are used to set the output voltage of LDO3 as shown in Table 8.

Table 8 — LDO3 Control Codes

LDO3V3	LDO3V2	LDO3V1	LDO3V0	V_{LDO3}
0	0	0	0	OFF
0	0	0	1	3.3V
0	0	1	0	3.2V
0	0	1	1	3.1V
0	1	0	0	3.0V
0	1	0	1	2.9V
0	1	1	0	2.8V
0	1	1	1	2.7V
1	0	0	0	2.6V
1	0	0	1	2.5V
1	0	1	0	2.4V
1	0	1	1	2.2v
1	1	0	0	1.8V
1	1	0	1	1.7V
1	1	1	0	1.6V
1	1	1	1	1.5V

Register Map (continued)

LDO4 Control Register (08h)

This register is used to enable LDO4 and set its output voltage level.

Bits [D5:D4]

These bits are unused and are always zeroes.

LDO4V3 through LDO4V0 [D3:D0]

These bits are used to set the output voltage of LDO4 as shown in Table 9.

Table 9 — LDO4 Control Codes

LDO4V3	LDO4V2	LDO4V1	LDO4V0	V_{LDO4}
0	0	0	0	OFF
0	0	0	1	3.3V
0	0	1	0	3.2V
0	0	1	1	3.1V
0	1	0	0	3.0V
0	1	0	1	2.9V
0	1	1	0	2.8V
0	1	1	1	2.7V
1	0	0	0	2.6V
1	0	0	1	2.5V
1	0	1	0	2.4V
1	0	1	1	2.2V
1	1	0	0	1.8V
1	1	0	1	1.7V
1	1	1	0	1.6V
1	1	1	1	1.5V

Fade Control Register (09h)

This register contains the fade enables and rate controls for both the main display and sub display LED driver banks.

MFADE1 and MFADE0 [D2:D1]

These bits are used to set the rise/fall rate between two backlight currents for the main display as show in Table 10. For the fade feature to be active, the MFADE bit must be set. The number of steps required to change the backlight current will be equal to the change in binary count of bits MBL4 through MBL0.

Table 10 — Main Display Fade Control Bits

MFADE1	MFADE0	Fade Feature Rise/ Fall Rate (ms/step)
0	0	32
0	1	24
1	0	16
1	1	8

MFADE [D0]

This bit is used to enable or disable the fade feature. When MFADE is enabled and a new main backlight current is set, this current will change from its existing value to the new value written in MBL[4:0] at the rate determined by MFADE1 and MFADE0 (in ms/step). A new setting cannot be written during an ongoing fade operation, but an on-going fade operation may be cancelled by writing 0 to the MFADE bit. Clearing the MFADE bit during an ongoing fade operation changes the current immediately to the value of MBL[4:0]. The number of counts to complete a fade operation equals the difference between the old and new MBL[4:0] settings. If MFADE is cleared, the current level will change immediately without the fade delay. The rate of fade may be changed dynamically by writing new values to the MFADE1 and MFADE0 bits. The total fade time is given by the number of steps between old and new backlight values (see Table 4), multiplied by the rate of fade in ms/step.

Register Map (continued)

SFADE1 and SFADE0 [D5:D4]

These bits are used to set the rise/fall rate between two backlight currents for the sub display as show in Table 11. For the fade feature to be active, the SFADE bit must be set. The number of steps required to change the backlight current will be equal to the change in binary count of bits SBL4 through SBL0.

Table 11 — Sub Display Fade Control Bits

SFADE1	SFADE0	Fade Feature Rise/ Fall Rate (ms/step)
0	0	32
0	1	24
1	0	16
1	1	8

SFADE [D3]

This bit is used to enable or disable the fade feature. When SFADE is enabled and a new main backlight current is set, the current will change from its existing setting to the new setting written in SBL[4:0] at the rate determined by SFADE1 and SFADE0 (in ms/step). A new setting cannot be written during an ongoing fade operation, but an ongoing fade operation may be cancelled by writing 0 to the SFADE bit. Clearing the SFADE bit during an ongoing fade operation changes the current immediately to the value of SBL[4:0]. The number of counts to complete a fade operation equals the difference between the old and new SBL[4:0] settings. If SFADE is cleared, the current level will change immediately without the fade delay. The rate of fade may be changed dynamically by writing new values to the SFADE1 and SFADE0 bits. The total fade time is given by the number of steps between old and new backlight values (see Table 5), multiplied by the rate of fade in ms/step.

Bank Selection Register (0Ah)

This register contains the bits that determine which LED drivers are assigned to the main display and which are part of the sub display bank.

Bits [D5:D3]

These bits are unused and are always zeroes.

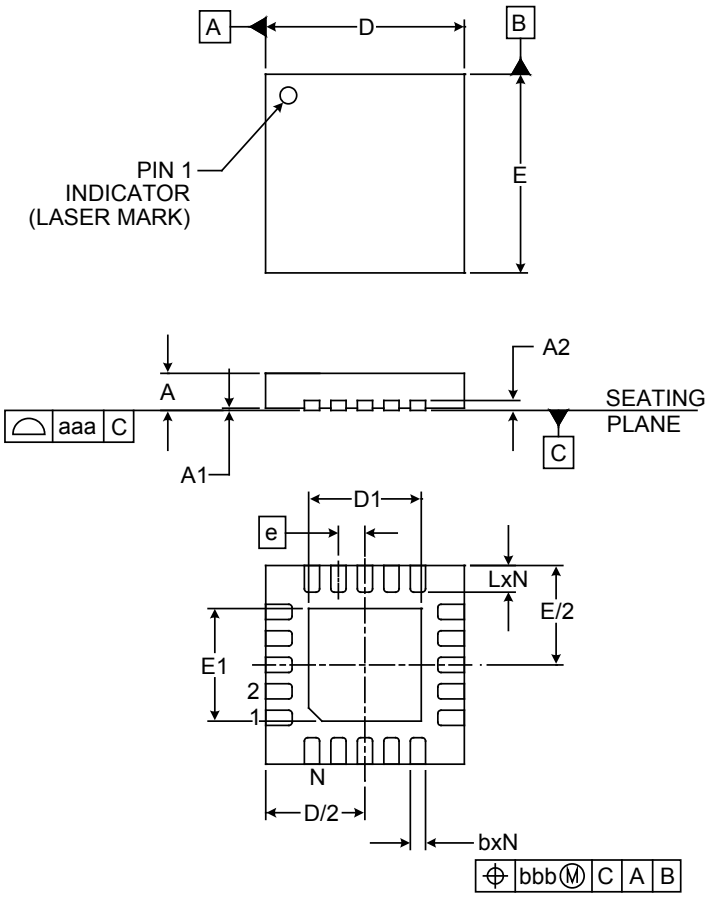
MB2, MB1, and MB0 [D2:D0]

These bits are used to set the number of LED drivers dedicated to a main backlight function. This allows the device to drive two different sets of LEDs with different settings for use in products like clamshell-style mobile phones that have a main display and a sub display with different lighting requirements. Note that any driver not selected for the main display will automatically be assigned to the sub display set. The code set by these three bits determines which LED drivers are dedicated to the main display according to the assignments listed in Table 12.

Table 12 — Main Display Driver Assignment Codes

MB2	MB1	MB0	Main Display Led Drivers	Sub Display LED Drivers
0	0	0	BL1 - BL6	none
0	0	1	BL1 - BL5	BL6
0	1	0	BL1 - BL4	BL5-BL6
0	1	1	BL1 - BL3	BL4 - BL6
1	0	0	BL1 - BL2	BL3 - BL6
1	0	1	BL1	BL2 - BL6
110 through 111			BL1 - BL6 (default)	none

Outline Drawing — MLPQ-UT-20 3x3

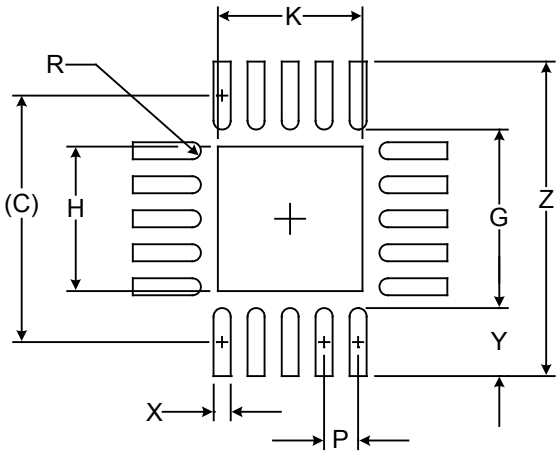


DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.020	-	.024	0.50	-	0.60
A1	.000	-	.002	0.00	-	0.05
A2		(.006)			(0.152)	
b	.006	.008	.010	0.15	0.20	0.25
D	.114	.118	.122	2.90	3.00	3.10
D1	.061	.067	.071	1.55	1.70	1.80
E	.114	.118	.122	2.90	3.00	3.10
E1	.061	.067	.071	1.55	1.70	1.80
e		.016 BSC			0.40 BSC	
L	.012	.016	.020	0.30	0.40	0.50
N		20			20	
aaa		.003			0.08	
bbb		.004			0.10	

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
3. DAP IS 1.90 x 1.90mm.

Land Pattern — MLPQ-UT-20 3x3



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.114)	(2.90)
G	.083	2.10
H	.067	1.70
K	.067	1.70
P	.016	0.40
R	.004	0.10
X	.008	0.20
Y	.031	0.80
Z	.146	3.70

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

Contact Information

Semtech Corporation
Power Management Products Division
200 Flynn Road, Camarillo, CA 93012
Phone: (805) 498-2111 Fax: (805) 498-3804

www.semtech.com