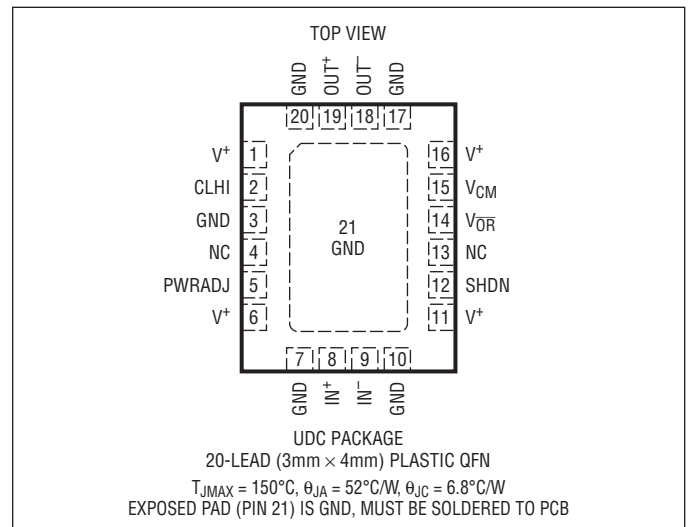


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to GND)	5.5V
Input Current (CLHI, V_{CM})	$\pm 10\text{mA}$
Input Current (IN^+ , IN^-)	$\pm 30\text{mA}$
Output Current (OUT^+ , OUT^-)	$\pm 100\text{mA}$
Output Current (V_{OR})	$\pm 10\text{mA}$
Operating Temperature Range	
(T_C) (Note 2)	-40°C to 105°C
Specified Temperature Range	
(T_C) (Note 3)	-40°C to 105°C
Storage Temperature Range	-65°C to 150°C
Junction Temperature (T_{JMAX})	150°C

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC6417CUDC#PBF	LTC6417CUDC#TRPBF	LFVN	20-Lead (3mm × 4mm) Plastic QFN	0°C to 70°C
LTC6417IUDC#PBF	LTC6417IUDC#TRPBF	LFVN	20-Lead (3mm × 4mm) Plastic QFN	-40°C to 105°C (T_C)

*Temperature grades are identified by a label on the shipping container.

Consult LTC Marketing for parts specified with wider operating temperature ranges.

Consult LTC Marketing for information on lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandree/>

DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V^+ = 5\text{V}$, GND = 0V, No R_{LOAD} , $C_{LOAD} = 6\text{pF}$. $V_{CM} = 1.25\text{V}$, CLHI = V^+ , PWRADJ = V^+ , SHDN = 0V unless otherwise noted. V_{INCM} is defined as $(IN^+ + IN^-)/2$. V_{OUTCM} is defined as $(OUT^+ + OUT^-)/2$. V_{INDIFF} is defined as $(IN^+ - IN^-)$. $V_{OUTDIFF}$ is defined as $(OUT^+ - OUT^-)$. See DC test circuit schematic.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input/Output Characteristics						
G_{DIFF}	Differential Gain	$V_{INDIFF} = \pm 1.2\text{V}$ Differential	● -0.15 -0.2	-0.1	0 0	dB dB
TCG_{DIFF}	Differential Gain Temperature Coefficient		●	0.0002		dB/ $^\circ\text{C}$
$V_{SWINGDIFF}$	Differential Output Voltage Swing	$V_{OUTDIFF}$, $V_{INDIFF} = \pm 2.3\text{V}$	● 4 3.3	4.28		V_{P-P} V_{P-P}
$V_{SWINGMIN}$	Output Voltage Swing Low	Single-Ended Measurement of OUT^+ , OUT^- $V_{INDIFF} = \pm 2.3\text{V}$	●	0.19	0.28 0.4	V V
$V_{SWINGMAX}$	Output Voltage Swing High	Single-Ended Measurement of OUT^+ , OUT^- $V_{INDIFF} = \pm 2.3\text{V}$	●	2.25 2.05	2.33	V V

DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V^+ = 5\text{V}$, $\text{GND} = 0\text{V}$, No R_{LOAD} , $C_{\text{LOAD}} = 6\text{pF}$. $V_{\text{CM}} = 1.25\text{V}$, $\text{CLHI} = V^+$, $\text{PWRADJ} = V^+$, $\text{SHDN} = 0\text{V}$ unless otherwise noted. V_{INCM} is defined as $(\text{IN}^+ + \text{IN}^-)/2$. V_{OUTCM} is defined as $(\text{OUT}^+ + \text{OUT}^-)/2$. V_{INDIFF} is defined as $(\text{IN}^+ - \text{IN}^-)$. V_{OUTDIFF} is defined as $(\text{OUT}^+ - \text{OUT}^-)$. See DC test circuit schematic.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{OUT}	Output Current Drive (Notes 1, 4)	Single-Ended Measurement of OUT^+ , OUT^-	●	± 100			mA
V_{OS}	Differential Input Offset Voltage	$\text{IN}^+ = \text{IN}^- = 1.25\text{V}$, $V_{\text{OS}} = V_{\text{OUTDIFF}}/G_{\text{DIFF}}$	●	-3.2 -4	-0.1	3.2 4	mV mV
TCV_{OS}	Differential Input Offset Voltage Drift		●		1		$\mu\text{V}/^\circ\text{C}$
V_{IOCM}	Common Mode Offset Voltage, Input to Output	$V_{\text{OUTCM}} - V_{\text{INCM}}$	●	-120 -140	-60	-10 0	mV mV
IVR_{MIN}	Input Voltage Range, IN^+ , IN^- (Minimum) (Single-Ended)	Defined by Output Voltage Swing Test	●			0.1	V
IVR_{MAX}	Input Voltage Range IN^+ , IN^- (Maximum) (Single-Ended)	Defined by Output Voltage Swing Test	●	2.4			V
I_{B}	Input Bias Current, IN^+ , IN^-	$\text{IN}^+ = \text{IN}^- = 1.25\text{V}$	●	-13 -18	2	13 18	μA μA
R_{INDIFF}	Differential Input Resistance	$V_{\text{INDIFF}} = \pm 1.2\text{V}$	●	12 11	18.5	25 27.5	$\text{k}\Omega$ $\text{k}\Omega$
C_{INDIFF}	Differential Input Capacitance				1		pF
R_{INCM}	Input Common Mode Resistance	$\text{IN}^+ = \text{IN}^- = 0.65\text{V}$ to 1.85V	●	5.8 5	9.25	13 15	$\text{k}\Omega$ $\text{k}\Omega$
CMRR	Common Mode Rejection Ratio	$\text{IN}^+ = \text{IN}^- = 0.65\text{V}$ to 1.85V , $\text{CMRR} = (V_{\text{OUTDIFF}}/G_{\text{DIFF}}/1.2\text{V})$	●	63 60	91		dB dB
R_{OUTDIFF}	Differential Output Resistance				3		Ω
e_{N}	Input Noise Voltage Density	$f = 100\text{kHz}$			1.5		$\text{nV}/\sqrt{\text{Hz}}$
i_{N}	Input Noise Current Density	$f = 100\text{kHz}$			4.3		$\text{pA}/\sqrt{\text{Hz}}$

Output Common Mode Voltage Control

G_{CM}	V_{CM} Pin Common Mode Gain	$V_{\text{CM}} = 0.65\text{V}$ to 1.85V	●	0.82 0.8	0.92		V/V V/V
$V_{\text{INCMDEFAULT}}$	Default Input Common Mode Voltage	V_{INCM} . IN^+ , IN^- , V_{CM} Pin Floating	●	1.15 1.1	1.25	1.35 1.4	V V
$V_{\text{OS}} (V_{\text{CM}} - V_{\text{INCM}})$	Offset Voltage, V_{CM} to V_{INCM}	$V_{\text{CM}} - V_{\text{INCM}}$, $V_{\text{CM}} = 1.25\text{V}$	●	-85 -90	15	115 135	mV mV
$V_{\text{OUTCMDEFAULT}}$	Default Output Common Mode Voltage	Inputs Floating, V_{CM} Pin Floating	●	1.1 1	1.2	1.3 1.35	V V
$V_{\text{OS}} (V_{\text{CM}} - V_{\text{OUTCM}})$	Offset Voltage, V_{CM} to V_{OUTCM}	$V_{\text{CM}} - V_{\text{OUTCM}}$, $V_{\text{CM}} = 1.25\text{V}$	●	-50 -45	75	200 230	mV mV
V_{OUTCMMIN}	Output Common Mode Voltage Range (Minimum)	$V_{\text{CM}} = 0.1\text{V}$	●		0.29	0.63 0.65	V V
V_{OUTCMMAX}	Output Common Mode Voltage Range (Maximum)	$V_{\text{CM}} = 2.4\text{V}$	●	2 1.85	2.25		V V
$V_{\text{CMDEFAULT}}$	V_{CM} Pin Default Voltage		●	1.15 1.1	1.25	1.35 1.4	V V
R_{VCM}	V_{CM} Pin Input Resistance	$V_{\text{CM}} = 0.65\text{V}$ to 1.85V	●	2 1.9	2.7	3.4 3.7	$\text{k}\Omega$ $\text{k}\Omega$
C_{VCM}	V_{CM} Pin Input Capacitance				1		pF
I_{BVCM}	V_{CM} Pin Bias Current	$V_{\text{CM}} = 1.25\text{V}$	●	-15 -27.5	1	15 27.5	μA μA

DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V^+ = 5\text{V}$, $\text{GND} = 0\text{V}$, No R_{LOAD} , $C_{\text{LOAD}} = 6\text{pF}$. $V_{\text{CM}} = 1.25\text{V}$, $\text{CLHI} = V^+$, $\text{PWRADJ} = V^+$, $\text{SHDN} = 0\text{V}$ unless otherwise noted. V_{INCM} is defined as $(\text{IN}^+ + \text{IN}^-)/2$. V_{OUTCM} is defined as $(\text{OUT}^+ + \text{OUT}^-)/2$. V_{INDIFF} is defined as $(\text{IN}^+ - \text{IN}^-)$. V_{OUTDIFF} is defined as $(\text{OUT}^+ - \text{OUT}^-)$. See DC test circuit schematic.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC Clamping Characteristics							
$V_{\text{CLHIDEFAULT}}$	Default Output Clamp Voltage, High		●	2.4 2.35	2.48	2.55 2.6	V V
$V_{\text{OS}} (\text{CLHI} - V_{\text{OUTCM}})$	Offset Voltage, CLHI to V_{OUTCM}		●	-60 -85	20	80 85	mV mV
$V_{\text{OS}} (\text{CLLO} - V_{\text{OUT}})$	Offset Voltage, CLLO to V_{OUT}	$V_{\text{CLHI}} = 2.0\text{V}$, $V_{\text{CM}} = 1.25\text{V}$, $\text{IN}^+ = 2.4\text{V}$, $\text{IN}^- = 0.1\text{V}$	●	-100 -110	10	100 110	mV mV
G_{LOHI}	Low Side Clamp Gain with Respect to CLHI Pin	$V_{\text{CLHI}} = 2.0\text{V}$, $V_{\text{CM}} = 1.25\text{V}$, $\text{IN}^+ = 2.4\text{V}$, $\text{IN}^- = 0.1\text{V}$	●	-1.2 -1.25	-1	-0.8 -0.75	V/V V/V
G_{LOCM}	Low Side Clamp Gain with Respect to CM Pin	$V_{\text{CLHI}} = 2.0\text{V}$, $V_{\text{CM}} = 1.25\text{V}$, $\text{IN}^+ = 2.4\text{V}$, $\text{IN}^- = 0.1\text{V}$	●	1.65 1.5	1.9	2.2 2.25	V/V V/V
R_{CLHI}	CLHI Pin Input Resistance	$V_{\text{CLHI}} = 1.5\text{V}$ to 2.5V	●	3.4 3.1	4.8	5.7 6	k Ω k Ω
I_{BCLHI}	CLHI Pin Bias Current	$V_{\text{CLHI}} = 2.5\text{V}$	●	-12 -12.5	3	18 18.5	μA μA
Power Supply							
V_{S}	Supply Voltage Range		●	4.75		5.25	V
I_{S}	Supply Current		●	100 95	123	140 145	mA mA
PSRR	Power Supply Rejection Ratio	$V_{\text{S}} = 4.75\text{V}$ to 5.25V	●	65 63	72		dB dB
SHDN Pin							
I_{SHDN}	Shutdown Current	$V_{\text{SHDN}} = 5\text{V}$	●	17 15	24	29 35	mA mA
$V_{\text{SHDNDEFAULT}}$	Default Shutdown Voltage		●			0.1	V
$V_{\text{IL,SHDN}}$	SHDN Input Low Voltage		●			2	V
$V_{\text{IH,SHDN}}$	SHDN Input High Voltage		●	3.5			V
$I_{\text{IL,SHDN}}$	SHDN Input Low Current	$\text{SHDN} = 0\text{V}$	●	-1.6 -2	0	1.6 2	μA μA
$I_{\text{IH,SHDN}}$	SHDN Input High Current	$\text{SHDN} = 5\text{V}$	●	275 250	380	450 475	μA μA
C_{SHDN}	SHDN Pin Input Capacitance				1		pF
R_{SHDN}	SHDN Pin Input Resistance	$\text{SHDN} = 2.5\text{V}$ to 5V	●	6 5	10.5	14 15	k Ω k Ω
PWRADJ Pin							
$V_{\text{PWRADJDEFAULT}}$	Default PWRADJ Voltage	PWRADJ Floating		1.5 1.45	1.65	1.8 1.85	V V
$I_{\text{S,L}}$	Supply Low Current	PWRADJ = 0V	●	45 40	74	105 110	mA mA
$I_{\text{IL,PWRADJ}}$	PWRADJ Input Low Current	PWRADJ = 0V	●	-145 -165	-120	-80 -75	μA μA
$I_{\text{IH,PWRADJ}}$	PWRADJ Input High Current	PWRADJ = 5V	●	210 200	240	290 300	μA μA
C_{PWRADJ}	PWRADJ Pin Input Capacitance				1		pF

DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V^+ = 5\text{V}$, $\text{GND} = 0\text{V}$, No R_{LOAD} , $C_{\text{LOAD}} = 6\text{pF}$, $V_{\text{CM}} = 1.25\text{V}$, $\text{CLHI} = V^+$, $\text{PWRADJ} = V^+$, $\text{SHDN} = 0\text{V}$ unless otherwise noted. V_{INCM} is defined as $(\text{IN}^+ + \text{IN}^-)/2$. V_{OUTCM} is defined as $(\text{OUT}^+ + \text{OUT}^-)/2$. V_{INDIFF} is defined as $(\text{IN}^+ - \text{IN}^-)$. V_{OUTDIFF} is defined as $(\text{OUT}^+ - \text{OUT}^-)$. See DC test circuit schematic.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
R_{PWRADJ}	PWRADJ Pin Input Resistance	PWRADJ = 2.5V to 5.0V	●	10.5 10	14.5	19 20	k Ω k Ω
V_{OR} Pin							
$V_{\text{OR}}(\text{HI})$	Maximum Voltage on V_{OR} Pin	$V_{\text{CL}} = 5.0\text{V}$, $V_{\text{CM}} = 1.25\text{V}$	●	3.25 3.2	3.35	3.55 3.6	V V
$I_{\text{OR}}(\text{DEFAULT})$	Default Pull-Down Current on V_{OR} Pin	$V_{\text{CL}} = 50\text{V}$, $V_{\text{CM}} = 1.25\text{V}$	●	-900 -1150	-770	-650 -500	μA μA
$I_{\text{OR}}(\text{MAX})$	Maximum Pull-Down Current Both Clamps are Active	$V_{\text{CL}} = 2.0\text{V}$, $V_{\text{CM}} = 1.25\text{V}$, $\text{IN}^+ = 2.4\text{V}$, $\text{IN}^- = 0.1\text{V}$	●		1	1.5 2	μA μA

AC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V^+ = 5\text{V}$ unless otherwise noted, $\text{GND} = 0\text{V}$, $R_{\text{LOAD}} = 500\Omega$, $C_{\text{LOAD}} = 6\text{pF}$, $V_{\text{CM}} = 1.25\text{V}$, $\text{CLHI} = V^+$, $\text{PWRADJ} = V_{\text{CC}}$, $\text{SHDN} = 0\text{V}$ unless otherwise noted. V_{INCM} is defined as $(\text{IN}^+ + \text{IN}^-)/2$. V_{OUTCM} is defined as $(\text{OUT}^+ + \text{OUT}^-)/2$. V_{INDIFF} is defined as $(\text{IN}^+ - \text{IN}^-)$. V_{OUTDIFF} is defined as $(\text{OUT}^+ - \text{OUT}^-)$. See DC test circuit schematic.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Differential AC Characteristics							
-3dB BW	-3dB Bandwidth	200mV _{P-P,OUT} Differential			1.6		GHz
0.1dB BW	$\pm 0.1\text{dB}$ Bandwidth	200mV _{P-P,OUT} Differential			0.18		GHz
0.5dB BW	$\pm 0.5\text{dB}$ Bandwidth	200mV _{P-P,OUT} Differential			0.45		GHz
1/f	1/f Noise Corner				25		kHz
SR	Slew Rate	Differential			10		V/ns
$t_{\text{S}1\%}$	1% Settling Time	2V _{P-P,OUT}			0.8		ns
t_{OFF}	Shutdown Time	SHDN = 0V to 5V			40		ns
t_{ON}	Enable Time	SHDN = 5V to 0V			15		ns
$t_{\text{PWRADJ,OFF}}$	PWRADJ Off Time	PWRADJ = 5V to 0V			10		ns
$t_{\text{PWRADJ,ON}}$	PWRADJ On Time	PWRADJ = 0V to 5V			5		ns
$t_{\text{CL,OFF } 10\%}$	Clamp Release Time	CLHI = 1.5V, $V_{\text{CM}} = 1.25\text{V}$, $\text{IN}^+ = 1.625\text{V}$ to 1.25V, $\text{IN}^- = 1.25\text{V}$ to 0.875V			1		ns
$t_{\text{CL,ON } 10\%}$	Clamp Engage Time	CLHI = 1.5V, $V_{\text{CM}} = 1.25\text{V}$, $\text{IN}^+ = 1.25\text{V}$ to 1.625V, $\text{IN}^- = 1.25\text{V}$ to 0.875V			5		ns
Common Mode AC Characteristics (V_{CM} Pin)							
-3dB BW	V_{CM} Pin Small Signal -3dB BW	$V_{\text{CM}} = 0.1\text{V}_{\text{P-P}}$, Measured Single-Ended at Output			10		MHz
SR_{CM}	Common Mode Slew Rate	Measured Single-Ended at Output			2		V/ μs
Overrange AC Characteristics (V_{OR} Pin)							
-3dB BW	V_{OR} Pin Small Signal -3dB BW	$V_{\text{OR}} = 0.1\text{V}_{\text{P-P}}$, CLHI = 2V, $\text{IN}^+ = 2.4\text{V}$, $\text{IN}^- = 0.1\text{V}$, $R_{\text{VOR}} = 1\text{k}$, Measured Single-Ended at Output			200		MHz
SR_{VOR}	Overrange Slew Rate	Measured Single-Ended at Output			40		V/ μs
AC Clamping Characteristics							
t_{OVR}	Overdrive Recovery Time	1.9V _{P-P,OUT}			2		ns

AC ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V^+ = 5\text{V}$ unless otherwise noted, $\text{GND} = 0\text{V}$, $R_{\text{LOAD}} = 500\Omega$, $C_{\text{LOAD}} = 6\text{pF}$. $V_{\text{CM}} = 1.25\text{V}$, $\text{CLHI} = V^+$, $\text{PWRADJ} = V_{\text{CC}}$, $\text{SHDN} = 0\text{V}$ unless otherwise noted. V_{INCM} is defined as $(\text{IN}^+ + \text{IN}^-)/2$. V_{OUTCM} is defined as $(\text{OUT}^+ + \text{OUT}^-)/2$. V_{INDIFF} is defined as $(\text{IN}^+ - \text{IN}^-)$. V_{OUTDIFF} is defined as $(\text{OUT}^+ - \text{OUT}^-)$. See DC test circuit schematic.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
AC Linearity						
10MHz Signal						
HD3	Third Harmonic Distortion	$V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$, $R_L = 50\Omega$ $V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$		-89 -93		dBc dBc
IM3	Third Order Intermodulation Distortion	$V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$, $R_L = 50\Omega$ $V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$		-100 -110		dBc dBc
OIP3	Output Third Order Intercept	$V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$, $R_L = 50\Omega$		56		dBm
P1dB	Output 1dB Compression Point			16.1		dBm
70MHz Signal						
HD3	Third Harmonic Distortion	$V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$, $R_L = 50\Omega$ $V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$		-74 -77		dBc dBc
IM3	Third Order Intermodulation Distortion	$V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$, $R_L = 50\Omega$ $V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$		-86 -96		dBc dBc
OIP3	Output Third Order Intercept	$V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$, $R_L = 50\Omega$		48		dBm
P1dB	Output 1dB Compression Point			15.8		dBm
140MHz Signal						
HD3	Third Harmonic Distortion	$V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$, $R_L = 50\Omega$ $V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$		-69 -73		dBc dBc
IM3	Third Order Intermodulation Distortion	$V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$, $R_L = 50\Omega$ $V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$		-80 -91		dBc dBc
OIP3	Output Third Order Intercept	$V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$, $R_L = 50\Omega$		46		dBm
P1dB	Output 1dB Compression Point			15.8		dBm
200MHz Signal						
HD3	Third Harmonic Distortion	$V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$, $R_L = 50\Omega$ $V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$		-68 -71		dBc dBc
IM3	Third Order Intermodulation Distortion	$V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$, $R_L = 50\Omega$ $V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$		-78 -87		dBc dBc
OIP3	Output Third Order Intercept	$V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$, $R_L = 50\Omega$		44		dBm
P1dB	Output 1dB Compression Point			15.8		dBm
240MHz Signal						
HD3	Third Harmonic Distortion	$V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$, $R_L = 50\Omega$ $V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$		-67 -70		dBc dBc
IM3	Third Order Intermodulation Distortion	$V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$, $R_L = 50\Omega$ $V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$		-76 -85		dBc dBc
OIP3	Output Third Order Intercept	$V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$, $R_L = 50\Omega$		43		dBm
P1dB	Output 1dB Compression Point			15.7		dBm
300MHz Signal						
HD3	Third Harmonic Distortion	$V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$, $R_L = 50\Omega$ $V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$		-66 -69		dBc dBc

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
IM3	Third Order Intermodulation Distortion	$V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$, $R_L = 50\Omega$ $V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$		-73 -79		dBc dBc
OIP3	Output Third Order Intercept	$V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$, $R_L = 50\Omega$		41		dBm
P1dB	Output 1dB Compression Point			15.6		dBm

380MHz Signal

HD3	Third Harmonic Distortion	$V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$, $R_L = 50\Omega$ $V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$		-66 -68		dBc dBc
IM3	Third Order Intermodulation Distortion	$V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$, $R_L = 50\Omega$ $V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$		-68 -77		dBc dBc
OIP3	Output Third Order Intercept	$V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$, $R_L = 50\Omega$	36	39		dBm
P1dB	Output 1dB Compression Point			15.3		dBm

400MHz Signal

HD3	Third Harmonic Distortion	$V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$, $R_L = 50\Omega$ $V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$		-65 -68		dBc dBc
IM3	Third Order Intermodulation Distortion	$V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$, $R_L = 50\Omega$		-68		dBc
OIP3	Output Third Order Intercept	$V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$, $R_L = 50\Omega$		39		dBm
P1dB	Output 1dB Compression Point			15.3		dBm

500MHz Signal

HD3	Third Harmonic Distortion	$V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$, $R_L = 50\Omega$ $V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$		-65 -67		dBc dBc
IM3	Third Order Intermodulation Distortion	$V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$, $R_L = 50\Omega$		-64		dBc
OIP3	Output Third Order Intercept	$V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$, $R_L = 50\Omega$		37		dBm
P1dB	Output 1dB Compression Point			15.0		dBm

600MHz Signal

HD3	Third Harmonic Distortion	$V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$, $R_L = 50\Omega$		-60		dBc
IM3	Third Order Intermodulation Distortion	$V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$, $R_L = 50\Omega$		-58		dBc
OIP3	Output Third Order Intercept	$V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$, $R_L = 50\Omega$		34		dBm
P1dB	Output 1dB Compression Point			14.7		dBm

700MHz Signal

HD3	Third Harmonic Distortion	$V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$, $R_L = 50\Omega$		-55		dBc
IM3	Third Order Intermodulation Distortion	$V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$, $R_L = 50\Omega$		-52		dBc
OIP3	Output Third Order Intercept	$V_{\text{OUTDIFF}} = 2.4\text{V}_{\text{P-P}}$, $R_L = 50\Omega$		31		dBm
P1dB	Output 1dB Compression Point			14.2		dBm

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

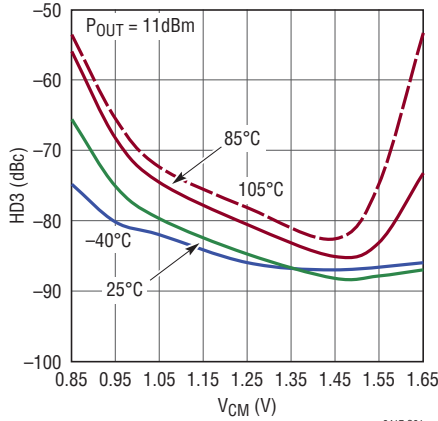
Note 2: The LTC6417C/LTC6417I is guaranteed functional over the case temperature operating range of -40°C to 105°C . $\theta_{\text{JC}} = 6.8^\circ\text{C/W}$.

Note 3: The LTC6417C is guaranteed to meet specified performance from 0°C to 70°C . It is designed, characterized and expected to meet specified performance from -40°C and 105°C case temperature range but is not tested or QA sampled at these temperatures. The LTC6417I is guaranteed to meet specified performance from -40°C to 105°C case temperature range.

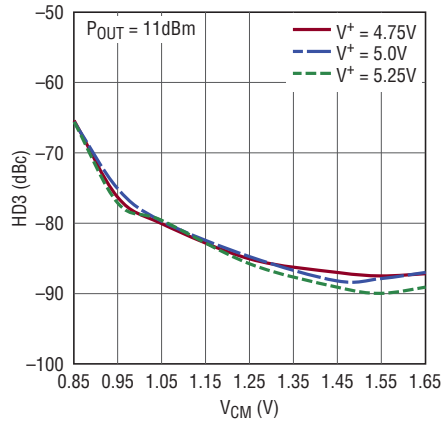
Note 4: This parameter is pulse tested.

TYPICAL PERFORMANCE CHARACTERISTICS

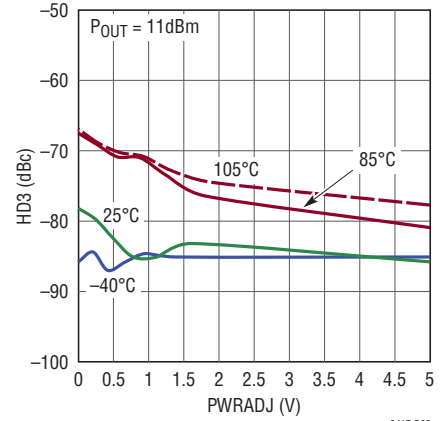
**HD3 at 30MHz
vs V_{CM} Over Temperature**



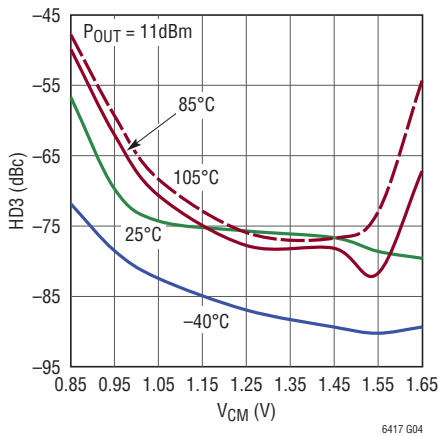
HD3 at 30MHz vs V_{CM} Over V^+



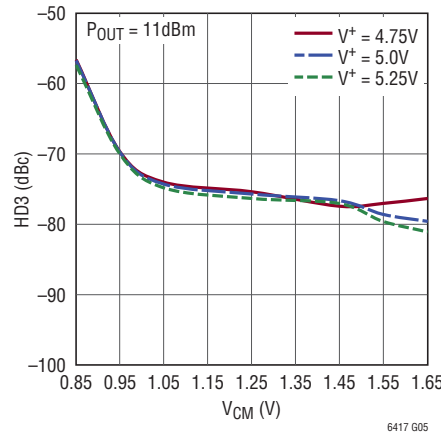
**HD3 at 30MHz
vs PWRADJ Over Temperature**



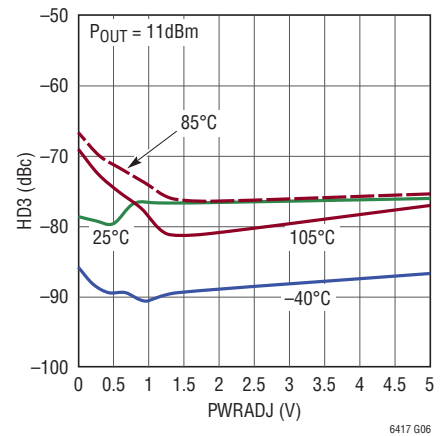
**HD3 at 70MHz
vs V_{CM} Over Temperature**



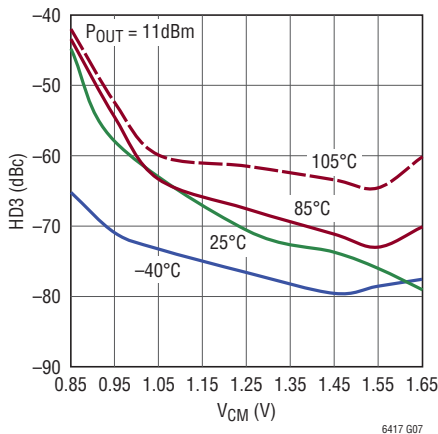
HD3 at 70MHz vs V_{CM} Over V^+



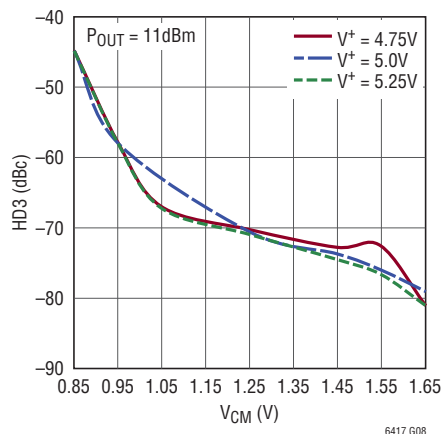
**HD3 at 70MHz
vs PWRADJ Over Temperature**



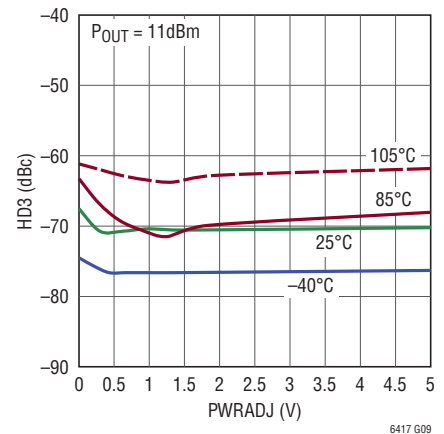
**HD3 at 140MHz
vs V_{CM} Over Temperature**



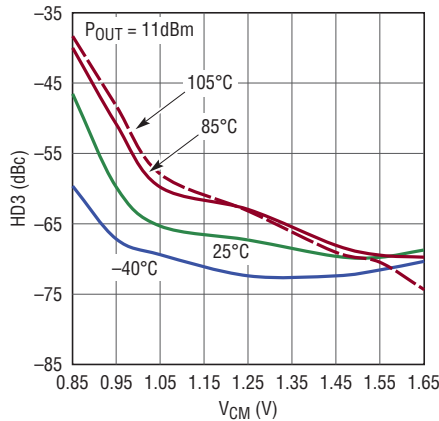
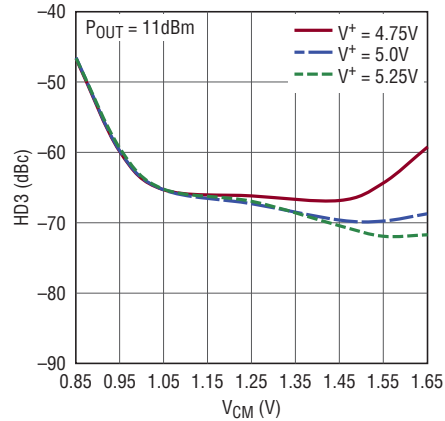
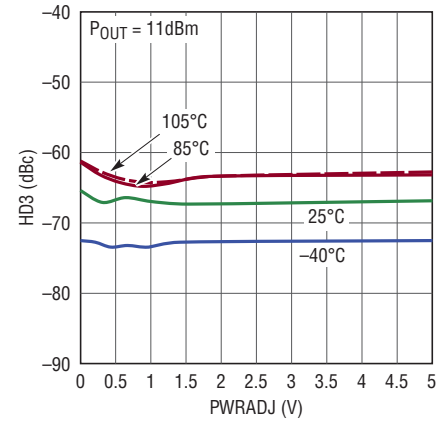
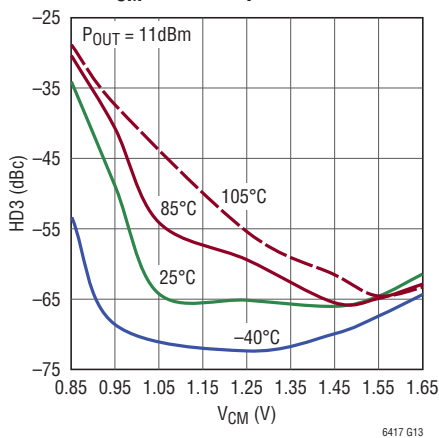
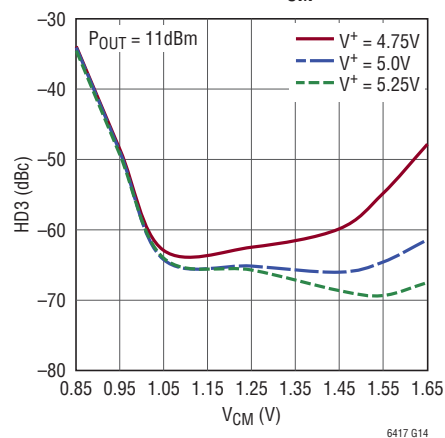
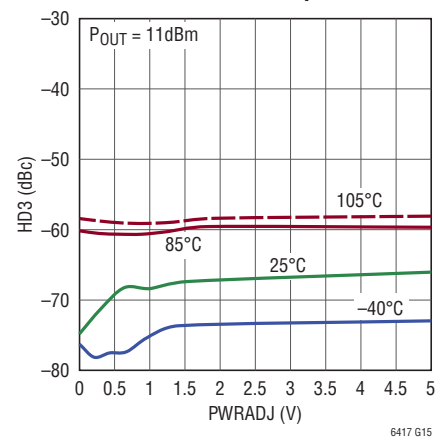
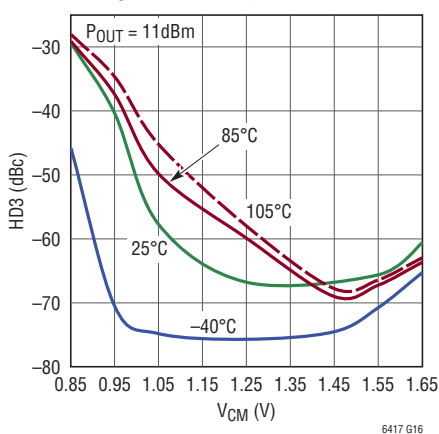
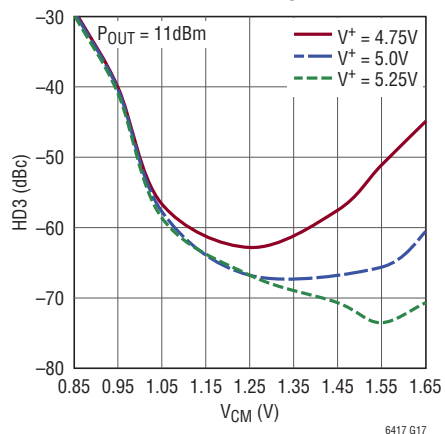
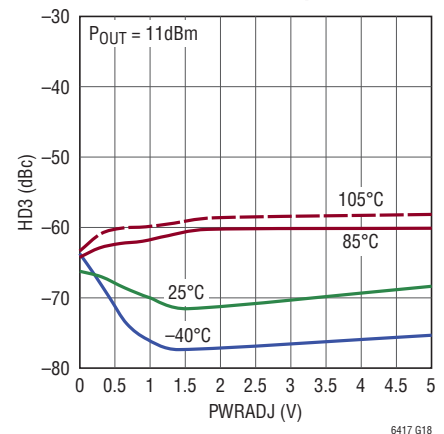
HD3 at 140MHz vs V_{CM} Over V^+



**HD3 at 140MHz
vs PWRADJ Over Temperature**

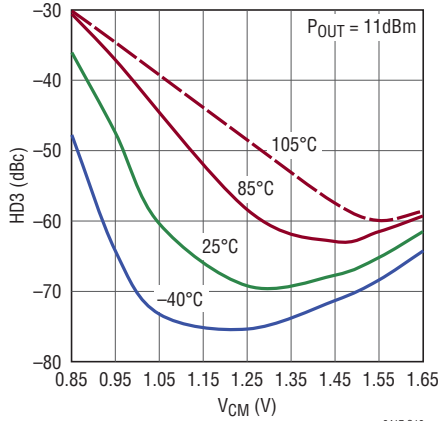


TYPICAL PERFORMANCE CHARACTERISTICS

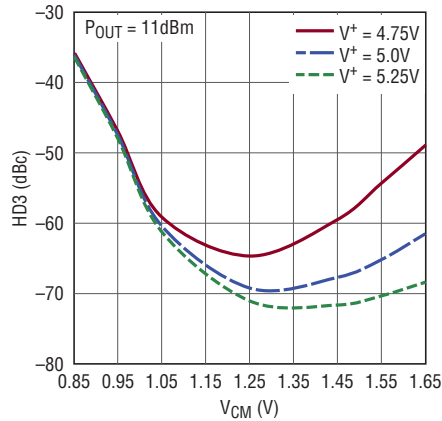
HD3 at 240MHz
vs V_{CM} Over TemperatureHD3 at 240MHz vs V_{CM} Over V^+ HD3 at 240MHz
vs PWRADJ Over TemperatureHD3 at 380MHz
vs V_{CM} Over TemperatureHD3 at 380MHz vs V_{CM} Over V^+ HD3 at 380MHz
vs PWRADJ Over TemperatureHD3 at 500MHz
vs V_{CM} Over TemperatureHD3 at 500MHz vs V_{CM} Over V^+ HD3 at 500MHz
vs PWRADJ Over Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

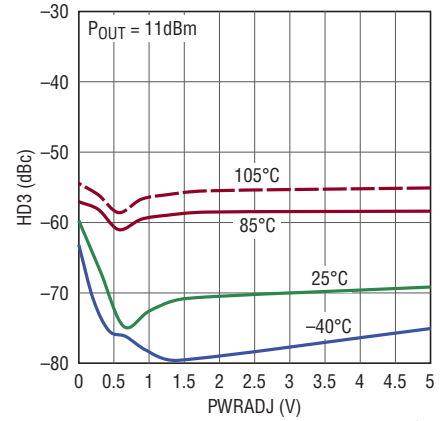
**HD3 at 600MHz
vs V_{CM} Over Temperature**



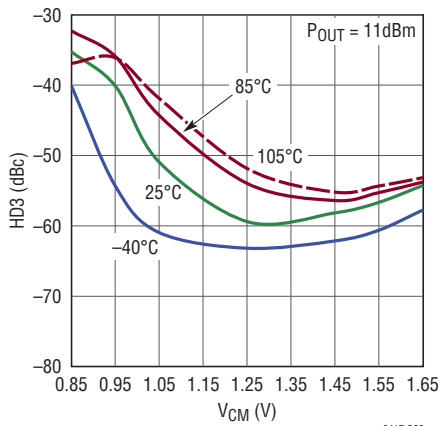
HD3 at 600MHz vs V_{CM} Over V^+



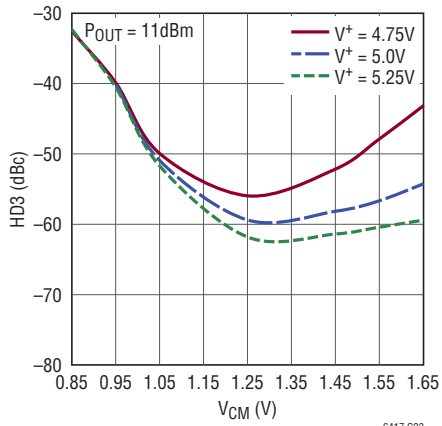
**HD3 at 600MHz
vs PWRADJ Over Temperature**



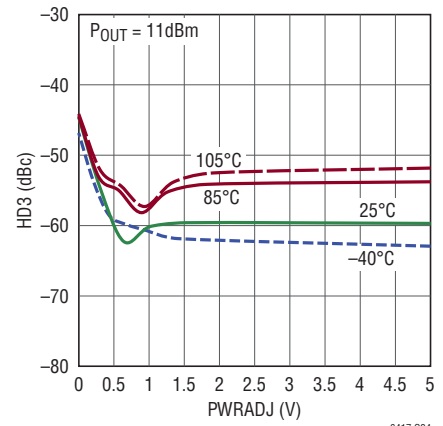
**HD3 at 700MHz
vs V_{CM} Over Temperature**



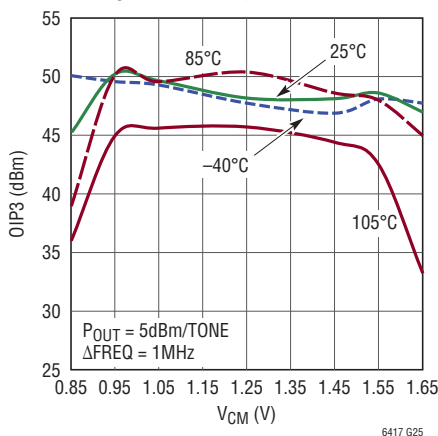
HD3 at 700MHz vs V_{CM} Over V^+



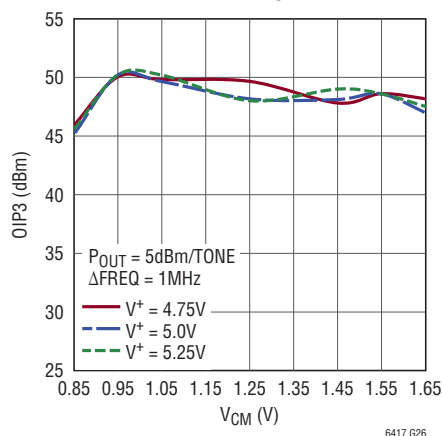
**HD3 at 700MHz
vs PWRADJ Over Temperature**



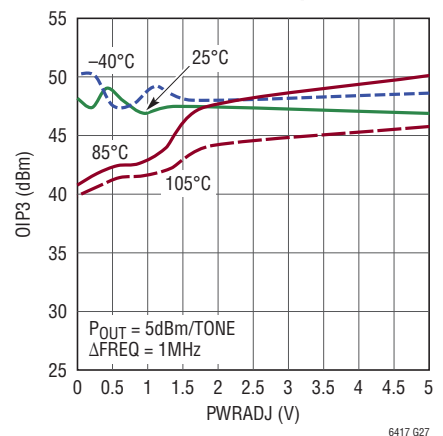
**OIP3 at 30MHz
vs V_{CM} Over Temperature**



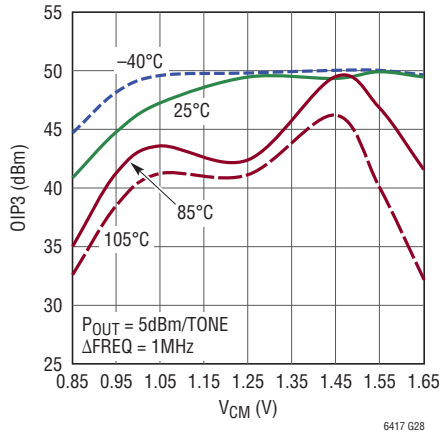
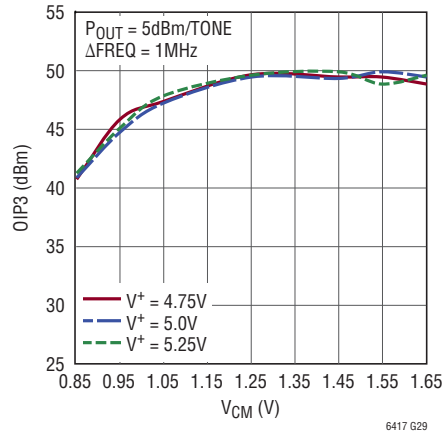
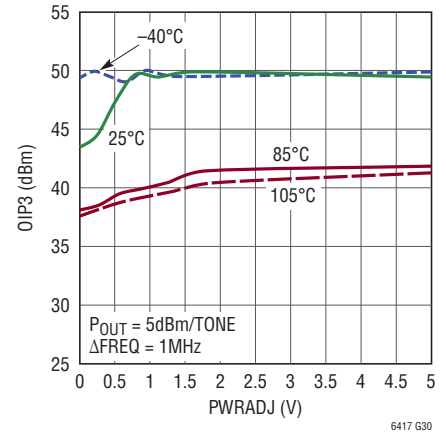
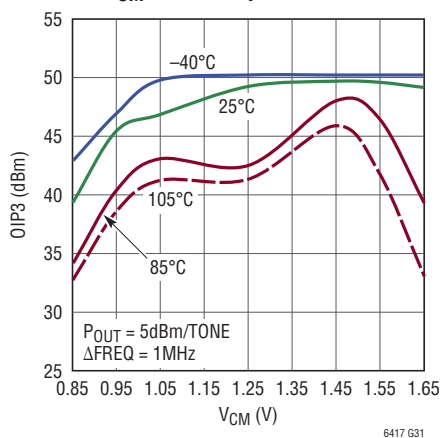
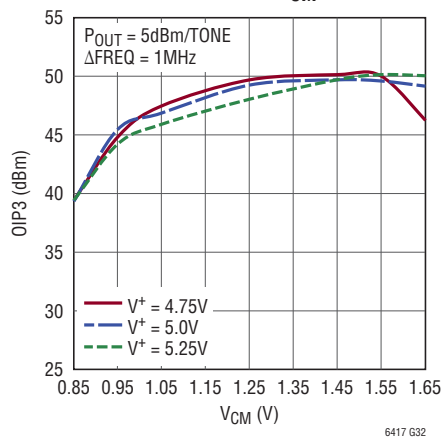
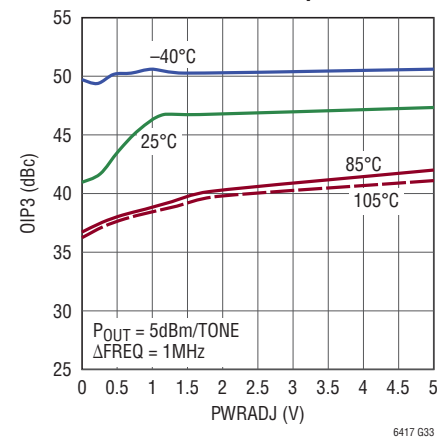
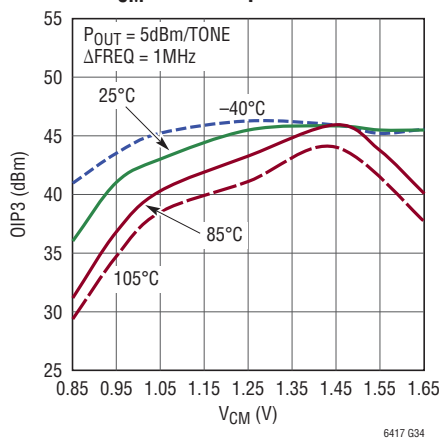
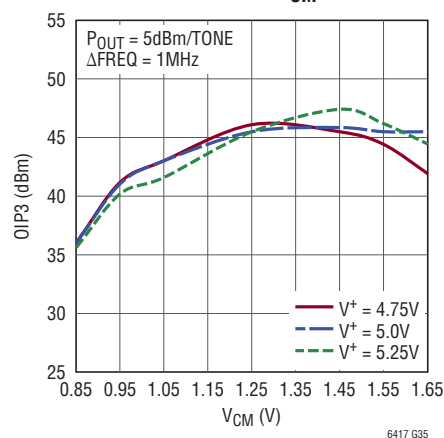
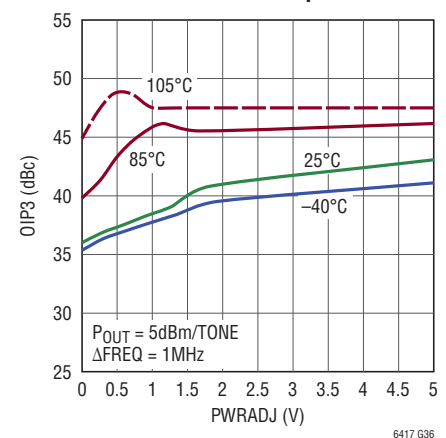
OIP3 at 30MHz vs V_{CM} Over V^+



**OIP3 at 30MHz
vs PWRADJ Over Temperature**

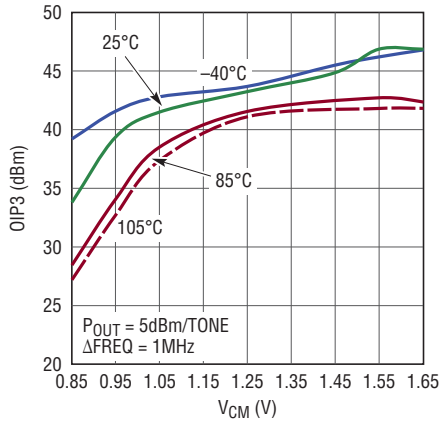


TYPICAL PERFORMANCE CHARACTERISTICS

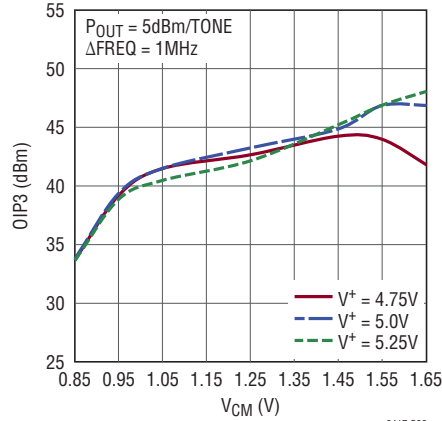
OIP3 at 70MHz
vs V_{CM} Over TemperatureOIP3 at 70MHz vs V_{CM} Over V^+ OIP3 at 70MHz
vs PWRADJ Over TemperatureOIP3 at 100MHz
vs V_{CM} Over TemperatureOIP3 at 100MHz vs V_{CM} Over V^+ OIP3 at 100MHz
vs PWRADJ Over TemperatureOIP3 at 140MHz
vs V_{CM} Over TemperatureOIP3 at 140MHz vs V_{CM} Over V^+ OIP3 at 140MHz
vs PWRADJ Over Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

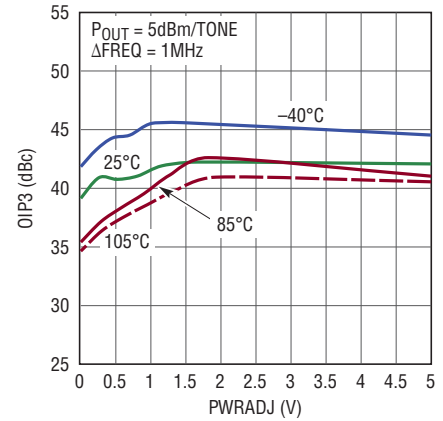
**OIP3 at 240MHz
vs V_{CM} Over Temperature**



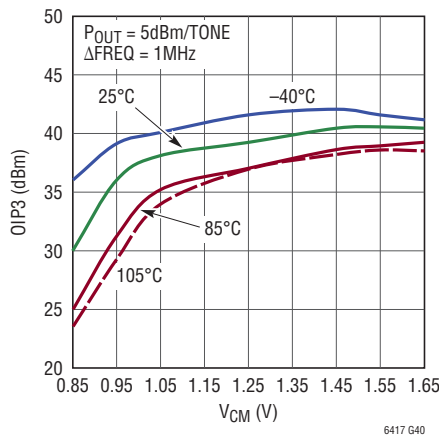
OIP3 at 240MHz vs V_{CM} Over V^+



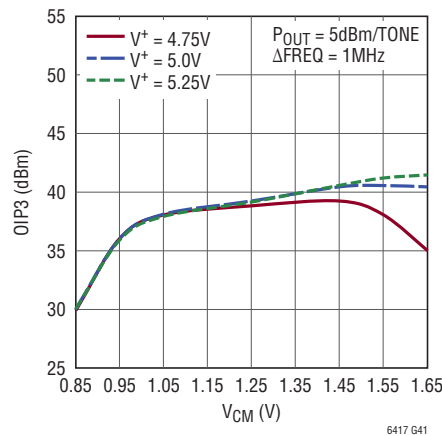
**OIP3 at 240MHz
vs PWRADJ Over Temperature**



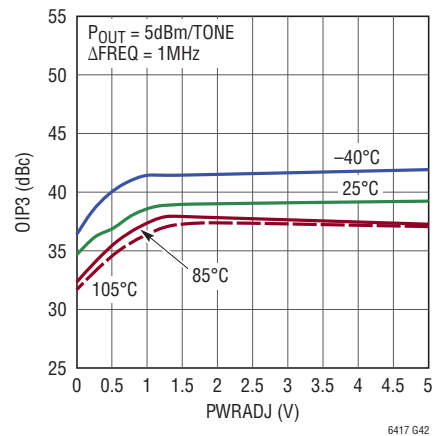
**OIP3 at 380MHz
vs V_{CM} Over Temperature**



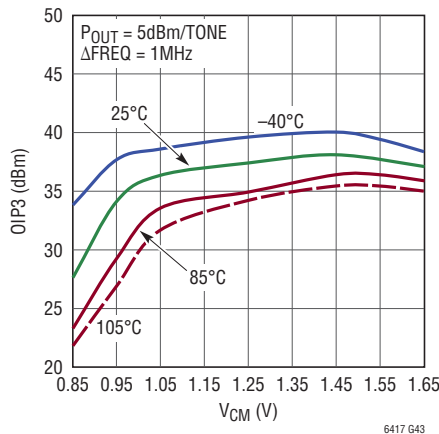
OIP3 at 380MHz vs V_{CM} Over V^+



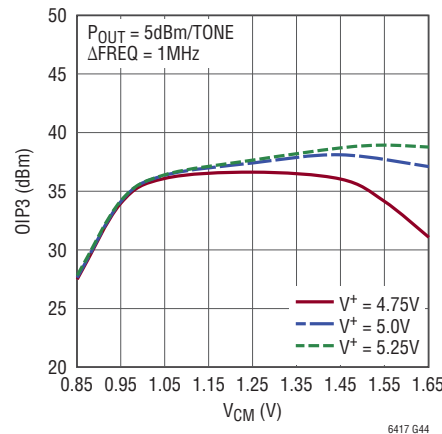
**OIP3 at 380MHz
vs PWRADJ Over Temperature**



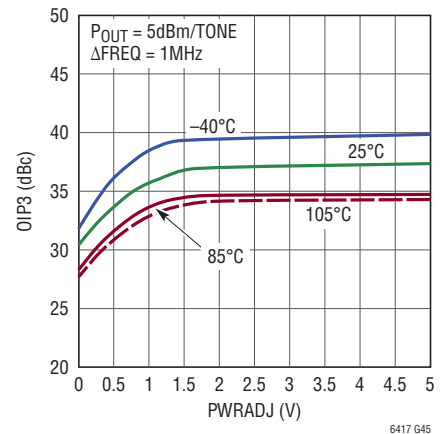
**OIP3 at 500MHz
vs V_{CM} Over Temperature**



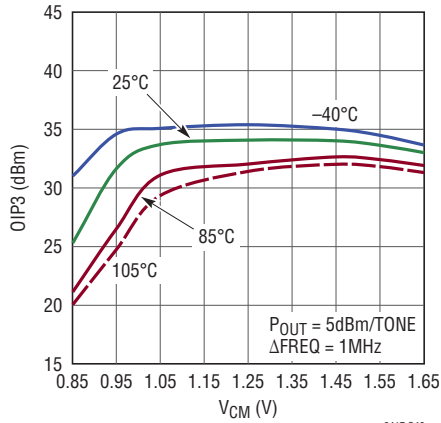
OIP3 at 500MHz vs V_{CM} Over V^+



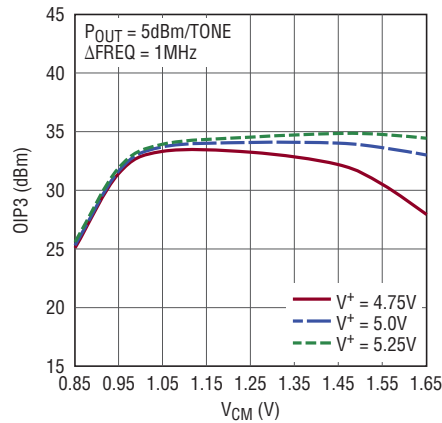
**OIP3 at 500MHz
vs PWRADJ Over Temperature**



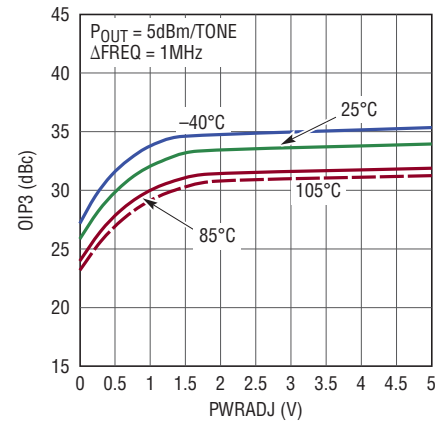
TYPICAL PERFORMANCE CHARACTERISTICS

OIP3 at 600MHz
vs V_{CM} Over Temperature

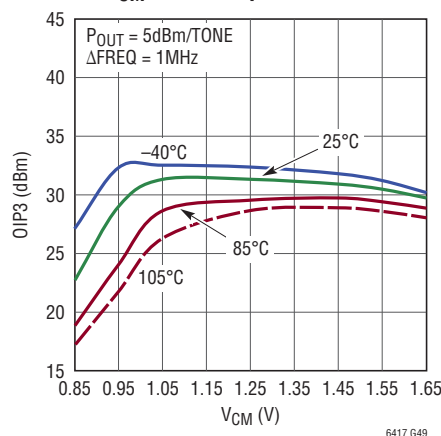
6417 G46

OIP3 at 600MHz vs V_{CM} Over V^+ 

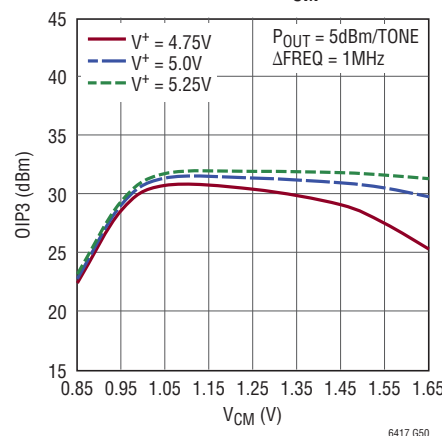
6417 G47

OIP3 at 600MHz
vs PWRADJ Over Temperature

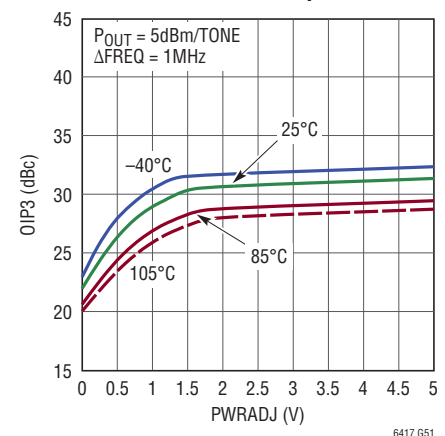
6417 G48

OIP3 at 700MHz
vs V_{CM} Over Temperature

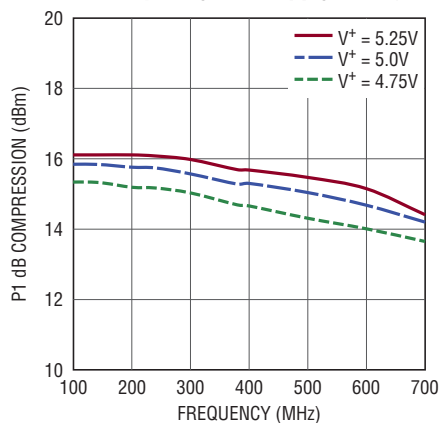
6417 G49

OIP3 at 700MHz vs V_{CM} Over V^+ 

6417 G50

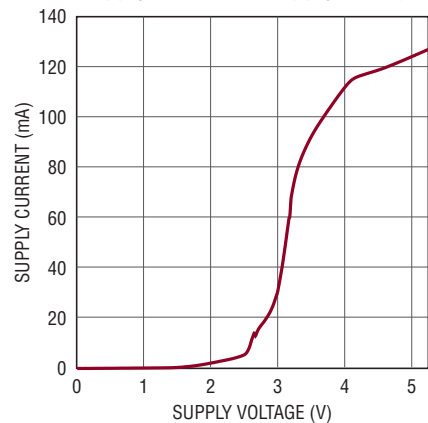
OIP3 at 700MHz
vs PWRADJ Over Temperature

6417 G51

Output 1dB Compression
vs Frequency and Supply Voltage

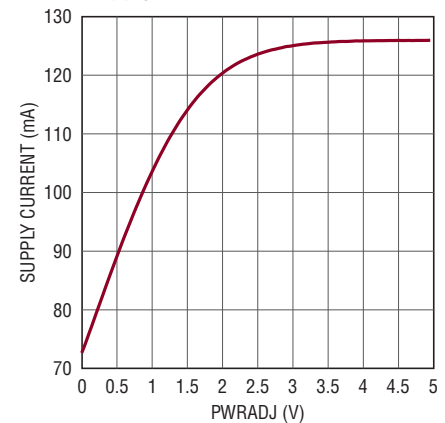
6417 G52

Supply Current vs Supply Voltage



6417 G53

Supply Current vs PWRADJ

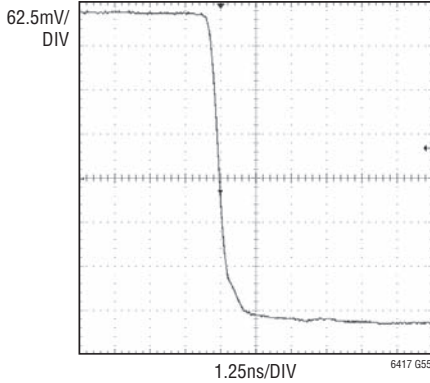


6417 G54

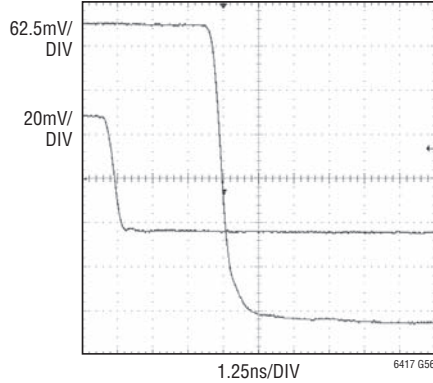
6417f

TYPICAL PERFORMANCE CHARACTERISTICS

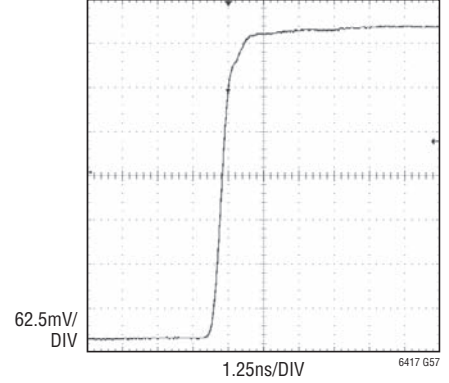
Small Signal Transient Response, Falling Edge



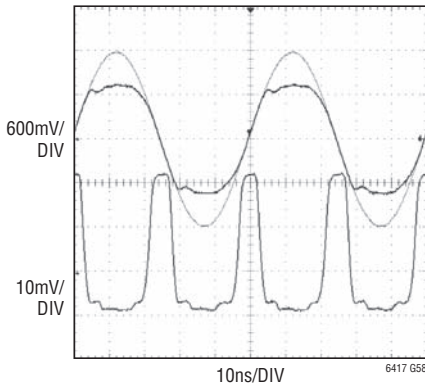
Small Signal Transient Response, Falling Edge with Input



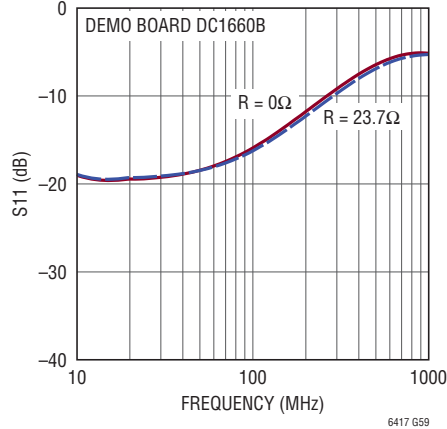
Small Signal Transient Response, Rising Edge



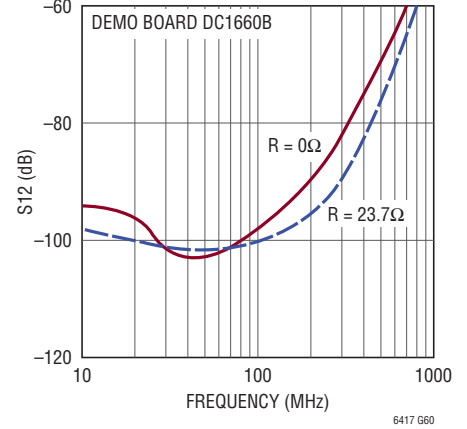
Overdrive Recovery and Overage Response



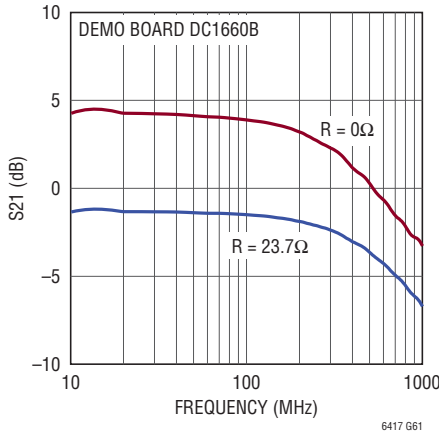
Differential Input Return Loss (S11) vs Frequency



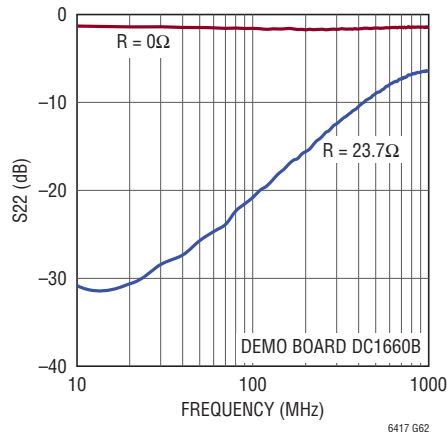
Differential Reverse Isolation (S12) vs Frequency



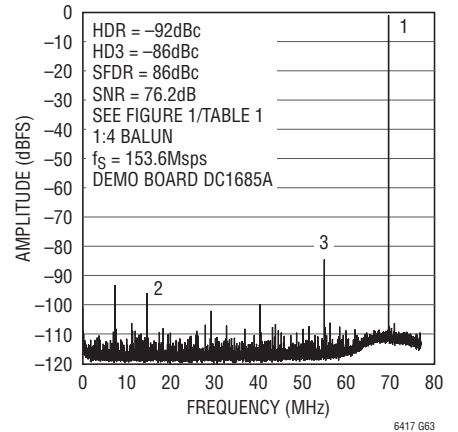
Differential Forward Gain (S21) vs Frequency



Differential Output Return Loss (S22) vs Frequency

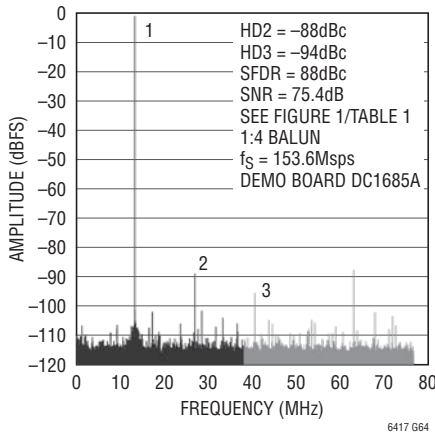


**LTC6417 Driving LTC2209
16-Bit ADC, 32K Point FFT,
 $f_{IN} = 69.5\text{MHz}$, -1dBFS , $\text{PGA} = 0$**

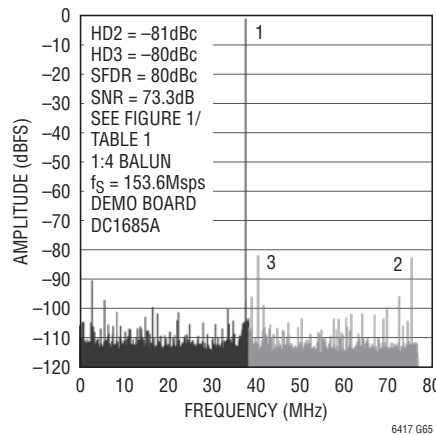


TYPICAL PERFORMANCE CHARACTERISTICS

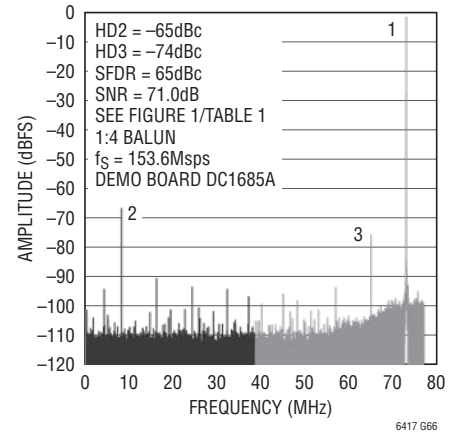
**LTC6417 Driving LTC2209
16-Bit ADC, 64K Point FFT,
 $f_{IN} = 140\text{MHz}$, -1dBFS , $\text{PGA} = 0$**



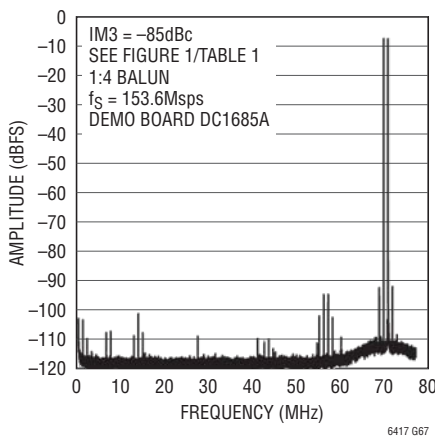
**LTC6417 Driving LTC2209
16-Bit ADC, 64K Point FFT,
 $f_{IN} = 270\text{MHz}$, -1dBFS , $\text{PGA} = 0$**



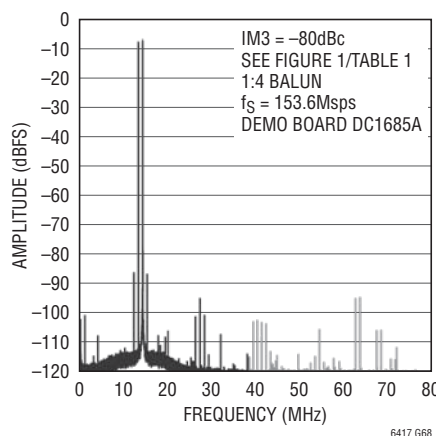
**LTC6417 Driving LTC2209
16-Bit ADC, 64K Point FFT,
 $f_{IN} = 380\text{MHz}$, -1dBFS , $\text{PGA} = 0$**



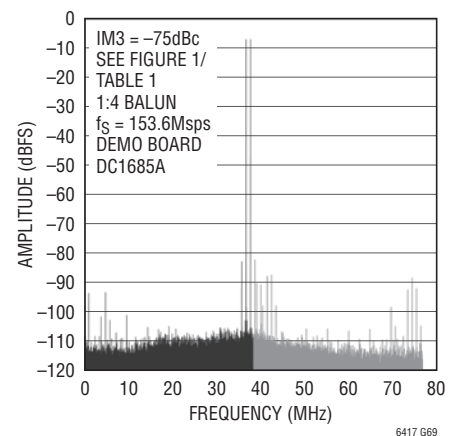
**LTC6417 Driving LTC2209 16-Bit ADC,
32K Point FFT, $f_{IN} = 69.5\text{MHz}$ and
 70.5MHz , -7dBFS/Tone , $\text{PGA} = 0$**



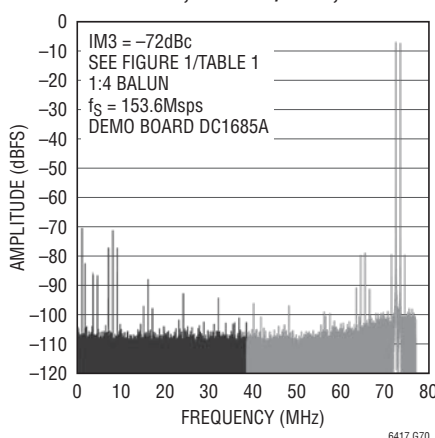
**LTC6417 Driving LTC2209 16-Bit ADC,
64K Point FFT, $f_{IN} = 139.5\text{MHz}$ and
 140MHz , -7dBFS/Tone , $\text{PGA} = 0$**



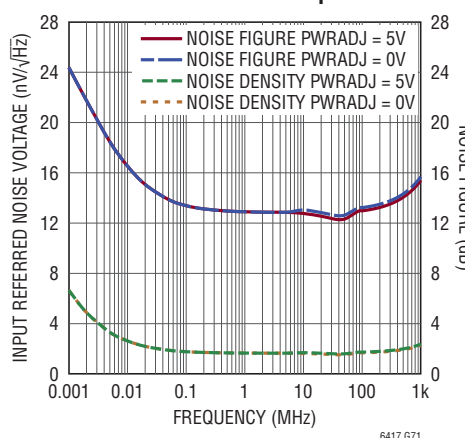
**LTC6417 Driving LTC2209 16-Bit ADC,
64K Point FFT, $f_{IN} = 269.5\text{MHz}$ and
 270.5MHz , -7dBFS/Tone , $\text{PGA} = 0$**



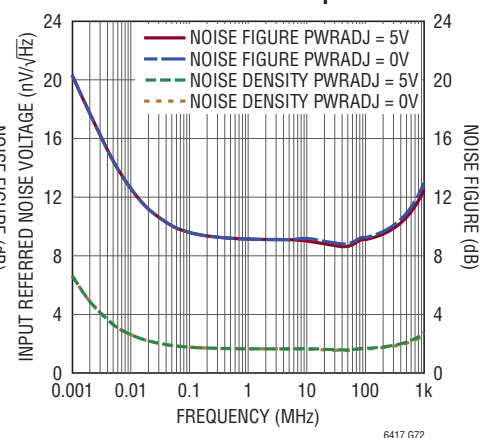
**LTC6417 Driving LTC2209 16-Bit ADC,
64K Point FFT, $f_{IN} = 379.5\text{MHz}$ and
 380.5MHz , -7dBFS/Tone , $\text{PGA} = 0$**



**Input Referred Noise Voltage
vs Frequency and Noise Figure for
the DC1660B with 1:1 Input Balun**



**Input Referred Noise Voltage
vs Frequency and Noise Figure for
the DC1660B with 1:4 Input Balun**



PIN FUNCTIONS

V⁺ (Pins 1, 6, 11, 16): Positive Power Supply. Typically 5V. Split supplies are possible as long as the voltage between V⁺ and GND is 4.75V to 5.25V. Bypass capacitors of 680pF and 0.1μF as close to the part as possible should be used between the supplies.

CLHI (Pin 2): High Side Clamp Voltage. The voltage applied to the CLHI pin defines the upper voltage limit of the OUT⁺ and OUT⁻ pins. This voltage should be set at least 300mV above the upper voltage range of the ADC. On a 5V supply, the CLHI pin will float to a 2.5V default voltage. CLHI has a Thevenin equivalent of approximately 4.8kΩ and can be overdriven by an external voltage. The CLHI pin should be bypassed with a high quality ceramic bypass capacitor of at least 0.01μF.

GND (Pins 3, 7, 10, 17, 20, Exposed Pad Pin 21): Negative Power Supply. Normally tied to ground. All pins and the exposed pad must be tied to the same voltage. GND may be tied to a voltage other than ground as long as the voltage between V⁺ and GND is 4.75V to 5.25V. If the GND pins are not tied to ground, bypass each with 680pF and 0.1μF capacitors as close to the package as possible. The exposed pad must be soldered to the printed circuit board ground plane for good heat transfer.

NC (Pins 4, 13): No Connection. These pins are not connected internally.

PWRADJ (Pin 5): Power Adjust Voltage. The voltage applied to this pin scales the bias current internal to the LTC6417. The PWRADJ pin will float to a 1.6V default voltage. PWRADJ has a Thevenin equivalent resistance of approximately 14.5k and can be overdriven by an external voltage. The PWRADJ pin should be bypassed with a high quality ceramic bypass capacitor of at least 0.01μF.

IN⁺, IN⁻ (Pin 8, Pin 9): Non-inverting and inverting input pins of the buffer, respectively. These pins are high impedance, approximately 9.5k. If AC-coupled, these pins will self bias to the voltage applied to the V_{CM} pin.

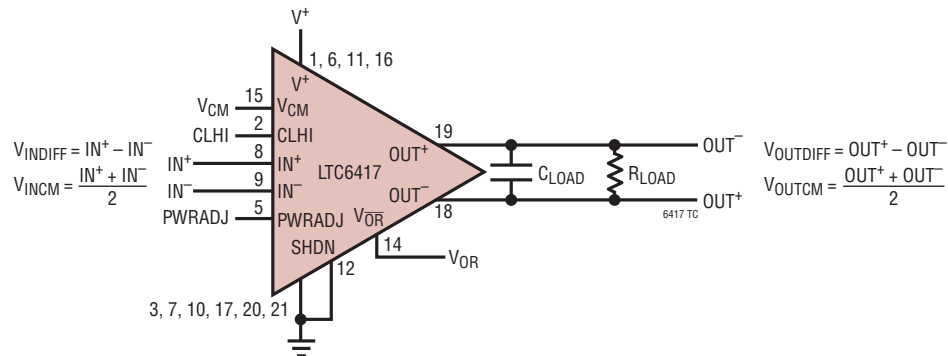
SHDN (Pin 12): This pin puts the LTC6417 in sleep mode when pulled high. If no voltage is applied to the SHDN pin, it floats down to the same potential as GND.

V_{OR} (Pin 14): Overrange Output. This pin, by default at 3.4V, will be pulled down to GND, when one or both input signals go beyond the minimum or maximum swing set by the CLHI and V_{CM} pins.

V_{CM} (Pin 15): This pin sets the output common mode voltage seen at OUT⁺ and OUT⁻ by driving IN⁺ and IN⁻ through a buffer with a high output resistance of 9.5k. The V_{CM} pin has a Thevenin equivalent resistance of approximately 2.7k and can be overdriven by an external voltage. If no voltage is applied to V_{CM}, it will float to a default voltage of approximately 1.25V on a 5V supply. The V_{CM} pin should be bypassed with a high quality ceramic bypass capacitor of at least 0.01μF.

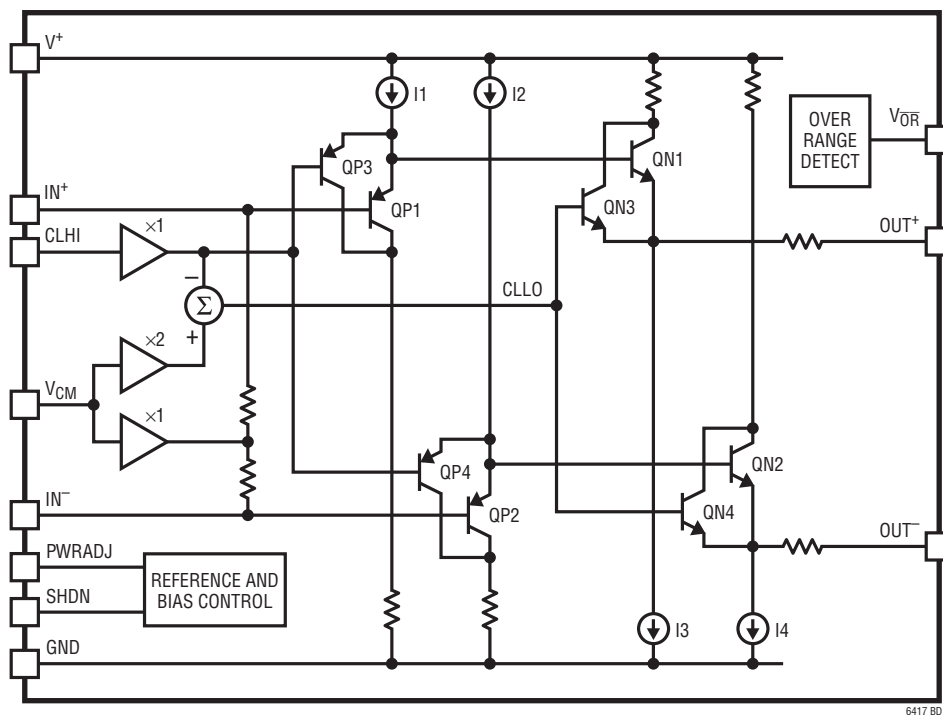
OUT⁻, OUT⁺ (Pin 18, Pin 19): Outputs.

DC TEST CIRCUIT SCHEMATIC



BLOCK DIAGRAM

LTC6417 Simplified Schematic



APPLICATIONS INFORMATION

Circuit Operation

The LTC6417 is a low noise and low distortion fully differential unity gain ADC driver with a -3dB bandwidth spanning DC to 1.6GHz , a differential input impedance of $18.5\text{k}\Omega$, and a differential output impedance of 3Ω . The LTC6417 is composed of a fully differential buffer with output common mode voltage control circuitry and high speed voltage-limiting clamps at the output. Lowpass or bandpass filters are easily implemented with just a few external components. The LTC6417 is very flexible in terms of I/O coupling. It can be AC- or DC-coupled at the inputs, the outputs or both. When using the LTC6417 with DC-coupled inputs, best performance is obtained with an input common mode voltage between 1V and 1.5V . For AC-coupled operation, the LTC6417 will take the voltage applied to the V_{CM} pin and use it to bias the inputs so that the output common mode voltage equals V_{CM} , thus no external circuitry is needed. The V_{CM} pin has been designed to directly interface with the V_{CM} pin found on Linear Technology's high speed ADC families.

Input Impedance and Matching

The LTC6417 has a high differential input impedance of $18.5\text{k}\Omega$. The differential inputs may need to be terminated to a lower value impedance, e.g. 50Ω , in order to provide an impedance match for the source. Figure 1 shows input matching and single-ended to differential conversion using a 1:1 balun, while Figure 2 shows a similar circuit using a 1:4 balun to achieve an additional 6dB of voltage gain. These circuits provide a wideband impedance match. The balun and matching resistors must be placed close to the input pins in order to minimize the rejection due to input mismatch. In Figures 1 and 2, the capacitor center-tapping the two input termination resistors improves high frequency common mode rejection. As an alternative to this wideband approach, a narrowband impedance match can be used at the inputs of the LTC6417 for frequency selection and/or noise reduction.

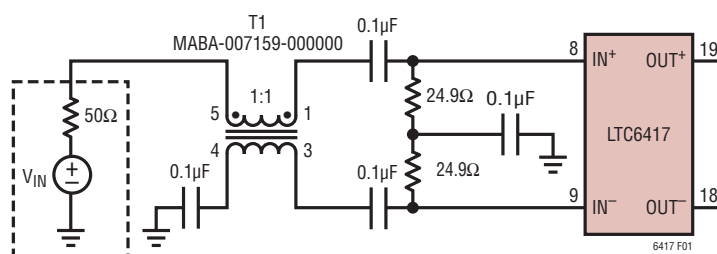


Figure 1. Input Termination for Differential 50Ω Input Impedance Using a 1:1 Balun

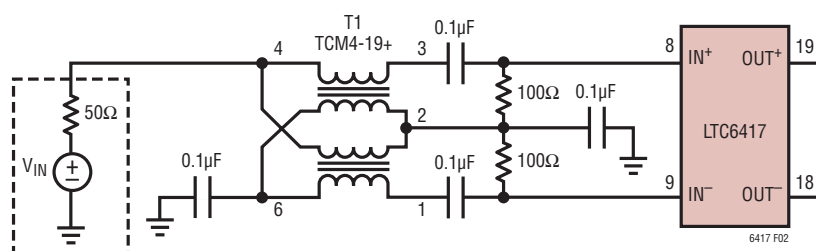


Figure 2. Input Termination for Differential 50Ω Input Impedance Using a 1:4 Balun

APPLICATIONS INFORMATION

The noise figure of the LTC6417 application circuit also depends upon the input termination. For example, the input 1:4 balun in Figure 2 improves noise figure by adding 6dB of voltage gain at the inputs. A trade-off between gain and noise is obvious when constant noise figure circle and constant gain circle are plotted within the same input Smith Chart. This technique can be used to determine the optimal source impedance for a given gain and noise requirement.

Output Match and Filter

The LTC6417 provides an output resistance of 1.5Ω at each output. In most cases, the LTC6417 can be used to drive an ADC without back termination but for testing purposes, Figure 3 shows the LTC6417 driving a differential 50Ω load impedance using a 1:1 balun. If output

matching for the 1:1 balun is desired, resistors of 23.7Ω should be inserted in series with each LTC6417 output. This is shown in Figure 4 where the LTC6417 is driving a differential 100Ω load impedance.

As mentioned above, the LTC6417 can drive an ADC without external output impedance matching, but improved performance can usually be obtained with the addition of a few components. Figure 5 shows a 6th order bandpass filter with a 148MHz center frequency, -3dB points of 85MHz and 210MHz used for driving the LTC2209 16-bit ADC. In the passband the filter has less than 1 dB ripple. This higher order filter has a sharp roll-off outside its passband, therefore it rejects noise and suppresses distortion components in its stopband. To double the filter center frequency, halve the capacitor and inductor values, and maintain resistor values; this also doubles the filter bandwidth.

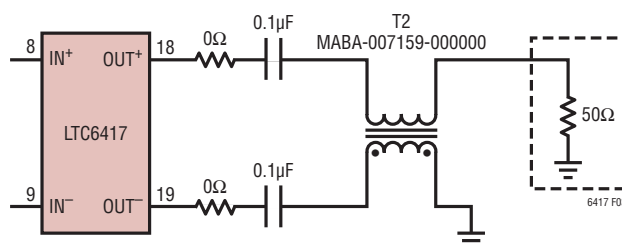


Figure 3. LTC6417 with No Back Termination Driving a 50Ω Load Using a 1:1 Balun

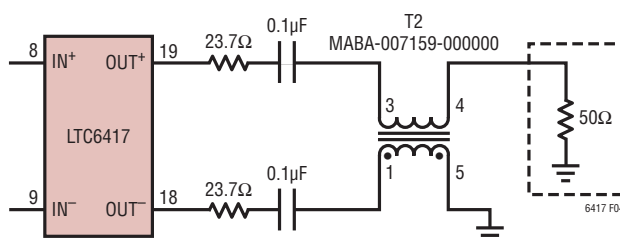


Figure 4. Output Termination for Differential 50Ω Load Using a 1:1 Balun

APPLICATIONS INFORMATION

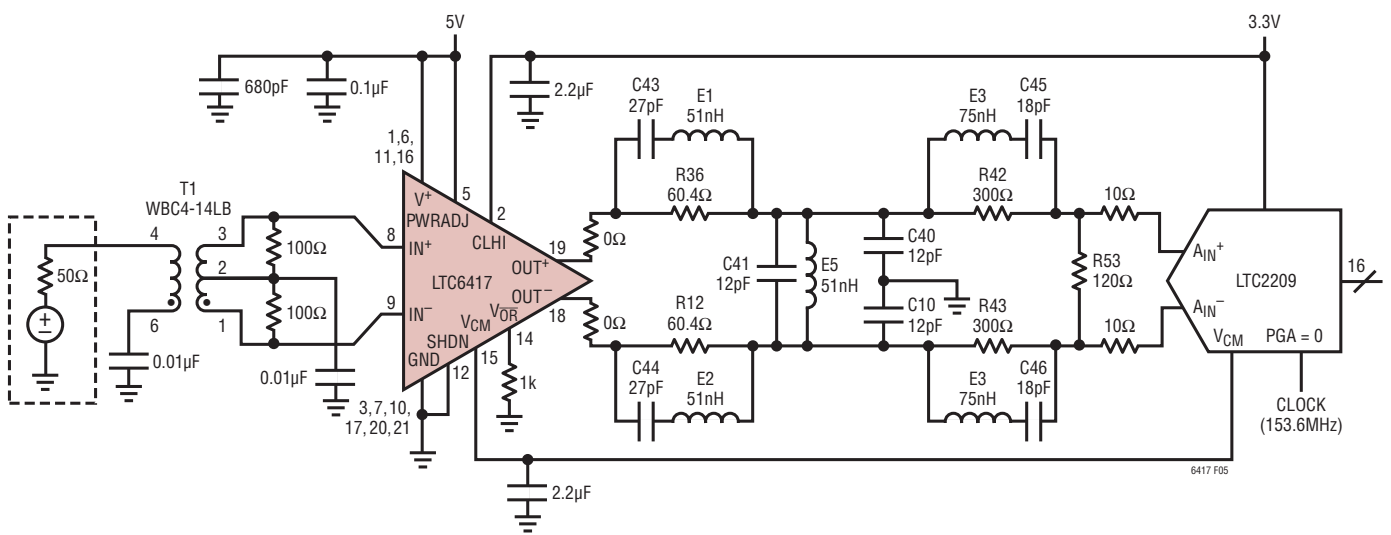


Figure 5. DC1685A Simplified Schematic with Suggested Bandpass Filter for Driving an LTC2209 16-Bit ADC at 140MHz

Table 1. Bandpass Filter Component Values for Different Input Frequencies

COMPONENTS	INPUT FREQUENCIES			
	70MHz	140MHz	270MHz	380MHz
R12 = R36	60.4Ω	60.4Ω	60.4Ω	60.4Ω
C43 = C44	56pF	27pF	15pF	12pF
E1 = E2	100nH	51nH	27nH	18nH
C41	47pF	12pF	12pF	10pF
C10 = C40	13pF	12pF	3.3pF	2.7pF
E5	100nH	51nH	27nH	18nH
R42 = R43	300Ω	300Ω	300Ω	300Ω
R53	120Ω	120Ω	120Ω	120Ω
C45 = C46	39pF	18pF	10pF	8.2pF
E3 = E4	150nH	75nH	39nH	27nH

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Output Common Mode Adjustment

For AC-coupled applications, the output common mode voltage is set by the V_{CM} pin. An internal buffer, as shown in Figure 6, couples the voltage on the V_{CM} pin to the inputs via high impedance resistors. Because the input common mode voltage is approximately the same as the output common mode voltage, both are approximately equal to the voltage applied to the V_{CM} pin. For DC-coupled applications, the internal V_{CM} is overdriven by the input signal. The V_{CM} pin has a Thevenin equivalent resistance of 2.7k and can be overdriven by an external voltage. The V_{CM} pin floats to a default voltage of 1.25V on a 5V supply. The output common mode voltage is capable of tracking V_{CM} in a range from 0.29V to 2.25V on a 5.0V supply. The V_{CM} pin can be floated, but it should always be bypassed close to the LTC6417 with a 0.1 μ F bypass capacitor to GND. When interfacing with A/D converters such as the LTC22xx families, the V_{CM} pin can be connected to the V_{CM} output pin of the ADC, as shown in Figure 5.

Clamping, the CLHI Pin and the V_{CM} Pin

The CLHI pin is used to set the high side clamp voltage of the high speed internal circuitry.

This limits the single-ended maximum and minimum voltage excursion at each of the outputs. This feature is extremely important in applications with input signals having very large peak-to-average ratios such as cellular base station receivers.

Internal circuitry generates a symmetric low side clamp voltage with respect to the common mode voltage V_{CM} (Figures 7 and 8). The LTC6417 clamp control circuitry features two additional mechanisms. First, internally imposed maximum swing of 2.5V and minimum swing of 0.2V ensure that the transistors do not go into deep saturation. This ensures a quick recovery after the clamps are released. Second, if CLHI voltage is less than V_{CM} , internal CLLO starts to track CLHI. This limits output swing and protects output transistors. Since the clamp response is on the order of 5ns to clamp and 1ns to release, clamp circuit becomes less effective at frequencies beyond 160MHz.

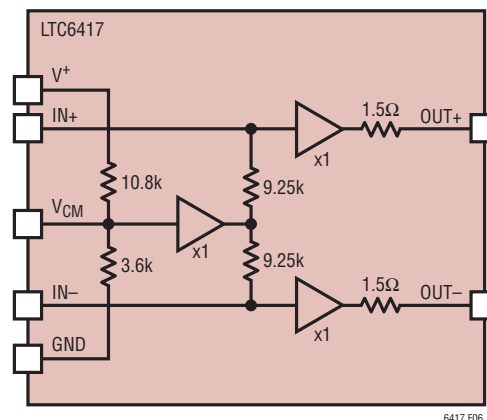


Figure 6. LTC6417 Internal Topology Showing the Common Mode Buffer Biasing the Inputs

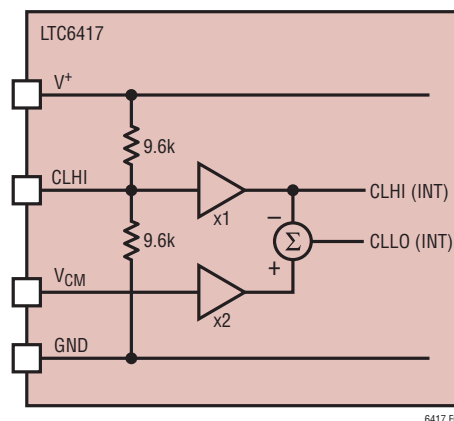


Figure 7. Internal Circuitry Generating Symmetric Clamp Voltages with Respect to V_{CM}

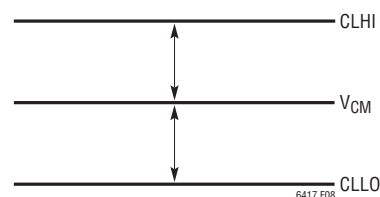


Figure 8. Symmetric High- and Low-Side Clamp Voltages with Respect to V_{CM}

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If a very large signal arrives at the LTC6417, the voltages applied to the CLHI and V_{CM} pins will determine the maximum and minimum output swing. Once the input signal returns to the normal operating range, the LTC6417 returns to linear operation within 2ns. For DC-coupled operation, the common mode of the input signals might be different than the voltage on the V_{CM} pin. The minimum swing will still be set by the voltages applied to the V_{CM} and CLHI pins.

CLHI is a high impedance input. It has an input impedance of 4.8k. On a 5V supply, CLHI self-biases to 2.5V. To limit the signal swing to a subsequent stage's power supply, e.g. an ADC such as the LTC2165, simply connect CLHI to the positive supply pin of the LTC2165. The CLHI pin should be bypassed with a 0.1 μ F capacitor as close to the LTC6417 as possible.

The V_{OR} Pin

The V_{OR} , overrange pin signals an overrange condition when one or both inputs exceed the minimum or maximum signal swing limits set by the CLHI and V_{CM} pins.

The LTC6417 V_{OR} pin can be used by a control system to limit the input power dynamically. This is very useful in applications where the overload response of the complete system would be too slow.

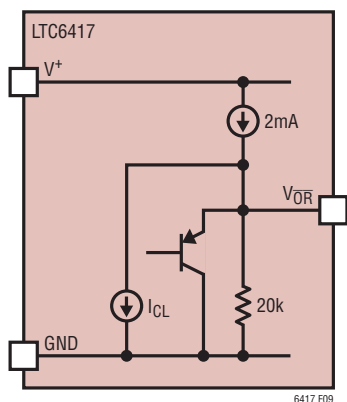


Figure 9. LTC6417 Internal Topology Showing V_{OR} Pin with Pull-Down Resistor and Clamp

The V_{OR} pin, as shown in Figure 9, is internally connected to a current source sourcing 2mA, plus an internal 20k resistor pull-down to GND. An internal clamp limits the maximum output to 3.4V. As soon as one of the inputs goes beyond the limits, and therefore engages one of the clamps, the output current, hence, the V_{OR} voltage goes to zero. The dynamic response of the V_{OR} pin can be adjusted with an external resistor and an optional external capacitor. For a high speed operation, add a 50 Ω resistor from V_{OR} to GND, resulting in a high speed signal with 100mV swing.

The PWRADJ Pin

The voltage applied to the PWRADJ pin scales the supply current and performance of the LTC6417. This is useful for reducing power consumption in applications where linearity of the LTC6417 exceeds the linearity of the other components in the system; hence LTC6417's linearity can be derated without effecting system performance. PWRADJ is a high impedance input. It has an input impedance of 14.5k. On a 5V supply, PWRADJ self-biases to 1.6V. For full power, simply connect PWRADJ to the positive supply V^+ . For minimum power, short the PWRADJ pin to GND. The PWRADJ pin should be bypassed with a 0.1 μ F capacitor as close to the LTC6417 as possible. LTC6417 performance vs PWRADJ can be found in the graphs.

The SHDN Pin

When pulled high, the SHDN pin puts the LTC6417 in sleep mode, significantly reducing supply current. SHDN is a high impedance input. It has an input impedance of 10.5k Ω . If the SHDN pin is not driven with an external voltage, it floats down to the same potential as GND, keeping the LTC6417 enabled. The SHDN pin should be bypassed with a 0.1 μ F capacitor as close to the LTC6417 as possible.

In sleep mode, the input and output stages are turned off, but the input and output clamps are kept alive to protect the part against overvoltage.

The supply current in sleep mode is only 24mA, instead of the typical 125mA. But should the clamps turn on, the current drawn from the supply can be as high as 180mA.

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This can be avoided by following a few precautions when putting the LTC6417 in sleep mode:

- Do not force the outputs below the inputs, this will turn the output stages on.
- Either float CLHI or tie it to V_{CC} . This will allow a wider signal range at the inputs before the clamps are activated.
- Maintain the inputs below CLHI or 2.5V whichever is lower, otherwise the input clamps will be activated.
- Do not short V_{CM} or the outputs to GND, in either case the output clamps will turn on. Current drawn from the supply can be as high as 180mA.
- Float the outputs if possible. The outputs will be pulled down by internal resistors to V_{CM} .

Heeding these precautions will protect the LTC6417 as well as any part it is driving, while maintaining a low current consumption in sleep mode.

Noise and Noise Figure

The LTC6417's differential input referred voltage and current noise densities are $1.5\text{nV}/\sqrt{\text{Hz}}$ and $4.3\text{pA}/\sqrt{\text{Hz}}$, respectively.

Before presenting a noise model, the circuit with the transformer in Figure 10 will be simplified. In Figure 11, the circuit is redrawn with the source impedance reflected to the secondary side of the transformer. The source impedance is multiplied by the impedance ratio m of the transformer. In Figure 12, noise sources associated with the amplifier and resistors have been added. Based on this noise model of the LTC6417, the total output noise power excluding the noise contribution of the source is:

$$\begin{aligned} e_{no}^2 &= e_{ni}^2 + (i_{ni} \cdot R_{EQ})^2 + i_{RT}^2 \cdot R_{EQ}^2 \\ &= e_{ni}^2 + (i_{ni} \cdot R_{EQ})^2 + \frac{4kT}{R_T} \cdot R_{EQ}^2 \end{aligned}$$

where $R_{EQ} = mR_S || R_T$ is the equivalent impedance seen at the input of the LTC6417. The output noise power due to the noise of source resistance is given by:

$$\begin{aligned} e_{no(mR_S)}^2 &= i_{mR_S}^2 \cdot R_{EQ}^2 \\ &= \frac{4kT}{mR_S} \cdot R_{EQ}^2 \end{aligned}$$

Noise figure (NF) is calculated from the ratio of these noise powers:

$$NF = 10 \log \left(1 + \frac{e_{no}^2}{e_{no(mR_S)}^2} \right)$$

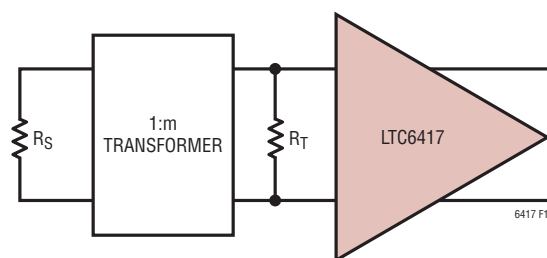


Figure 10. LTC6417 with a Transformer

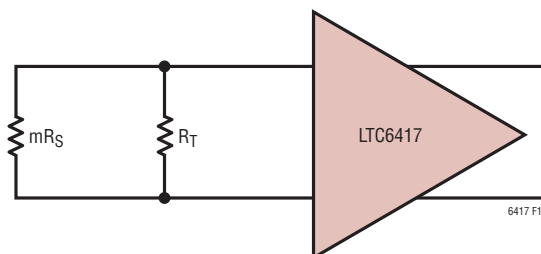


Figure 11. Source Resistance Referred to the Secondary

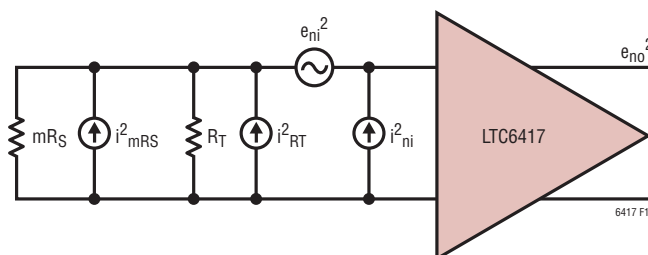


Figure 12. LTC6417 Simplified Noise Model

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In most cases the termination resistor will be matched to the source resistance, e.g. $R_T = mR_S$. For the LTC6417 with a wide-band terminated transformer, a plot of output and input noise density and NF versus termination resistor is shown in Figure 13. To get the best noise performance in the system, use the LTC6417 matched to a transformer with high impedance ratio. Although the output noise density will be higher, noise figure will improve because of the additional gain realized in the transformer. An impedance ratio greater than 8 is not recommended, as the increased termination resistance with the LTC6417 input capacitance will limit signal bandwidth. Consult Table 2 for a quick estimate of the LTC6417's output noise density and NF for different transformer impedance ratios. Measured NF numbers will be higher as the simple noise model does not take the insertion loss in the transformer into account.

Table 2. Output Noise Density and NF of the LTC6417 with a Wide-Band Terminated Transformer, $R_S = 50\Omega$

TRANSFORMER IMPEDANCE RATIO m	TERMINATION RESISTOR R_T (Ω)	GAIN (V/V)	OUTPUT NOISE DENSITY e_{no} ($nV/\sqrt{Hz}$)	NF (dB)
1	50	1.0	1.57	11.2
2	100	1.4	1.64	8.9
4	200	2.0	1.80	7.0
8	400	2.8	2.14	5.9

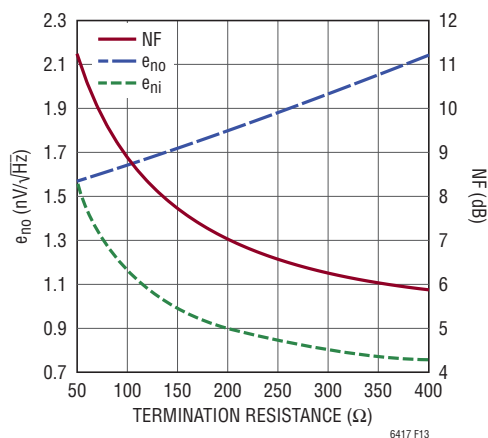


Figure 13. LTC6417 Output and Input Noise Density and NF vs Termination Resistance

Interfacing the LTC6417 to A/D Converters

The LTC6417 has been specially designed to interface directly with high speed A/D converters. It is possible to drive the ADC directly from the LTC6417. In practice, however, better performance may be obtained by adding a few external components at the output of the LTC6417. Figure 5 shows the LTC6417 driving an LTC2209 16-bit ADC. The differential outputs of the LTC6417 are bandpass filtered, then drive the differential inputs of the LTC2209. In many applications, a filter like this is desirable to limit the wideband noise of the amplifier. This is especially true in high performance 16-bit designs. The minimum recommended network between the LTC6417 and the ADC is simply two 10Ω series resistors, which are used to help eliminate resonances associated with the stray capacitance of PCB traces and the stray inductance of the internal bond wires at the ADC input pins and the driver output pins.

Single-Ended Signals

The LTC6417 has not been designed to convert single-ended signals to differential signals. A single-ended input signal can be converted to a differential signal via a balun connected to the inputs of the LTC6417. Figure 5 shows the LTC6417 driven by a 1:4 transformer which provides 6dB of voltage gain while also performing a single-ended to differential conversion.

Power Supply Considerations

For best linearity, the LTC6417 should have a positive supply of $V^+ = 5V$. For ESD protection, the LTC6417 has an internal edge-triggered supply voltage clamp. The timing mechanism of the clamp enables the LTC6417's protection circuit during ESD events. This internal clamp can also be activated by voltage overshoot and rapid slew rate on the positive supply V^+ pin. The LTC6417 should not be hot-plugged into a powered socket because there is a risk of activating this internal ESD clamp circuit. Bypass capacitors of 680pF and 0.1 μ F should be connected to the V^+ pin, as close as possible to the LTC6417.

Interfacing the LTC6417 with Active Mixers for Ultrawide IF Bandwidth

The LTC6417 is an excellent interface amplifier for use with active downconverting mixers like the LTC5567. By using

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the LTC6417 as a post-amplifier for the LTC5567, it is possible to achieve IF bandwidths in excess of 500MHz, while adding bandpass filtering. A key to achieving this extremely wide IF bandwidth is the use of pre-emphasis inductors in series with the LTC6417 inputs to compensate for the inherent rolloff caused by the LTC6417 input capacitance interacting with the interface impedance. In the example seen in Figure 14, a value of 33nH for each pre-emphasis inductor gives excellent wideband performance. Figure 15 shows performance for various values of L. For L = 33nH, overall conversion gain remains within 1dB from 90MHz to 590MHz, resulting in 500MHz of IF bandwidth.

Test Circuits

Due to the fully differential design of the LTC6417 and its usefulness in applications both with and without ADCs, two test circuits have been used to generate the information in this data sheet. Test circuit A is DC1660B, a two-port

demonstration circuit for the LTC6417. The board layout and the schematic are shown in Figures 16 and 17. These circuits include a 1:4 input balun and a 1:1 output balun for single-ended-to-differential conversion, allowing direct analysis using a 2-port network analyzer. Including the input and output baluns, the -3dB bandwidth is approximately 600MHz. A 1:4 input balun before the LTC6417 inputs provides 6dB of voltage gain, but results in better noise figure performance compared to a 1:1 input balun. Noise figure measurements for both input baluns can be found in the graphs.

Test circuit B is DC1685A. It consists of an LTC6417 driving an LTC2209 16-bit 153.6MSPS ADC. It is intended for use in conjunction with DC890B (computer interface board) and proprietary Linear Technology evaluation software to evaluate the performance of both parts together. Both the DC1685A board layout and the schematic can be seen in Figures 18 and 19.

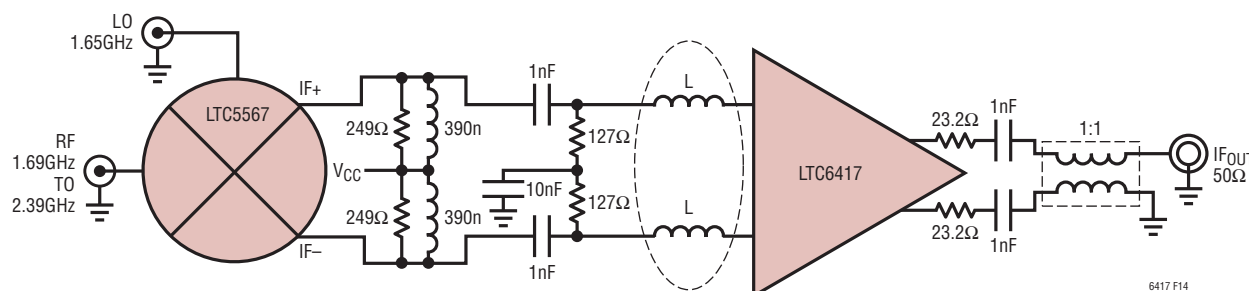


Figure 14

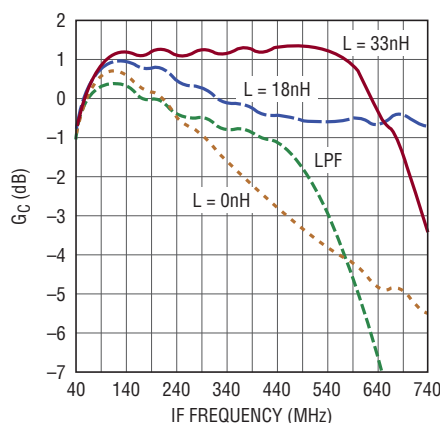


Figure 15

APPLICATIONS INFORMATION

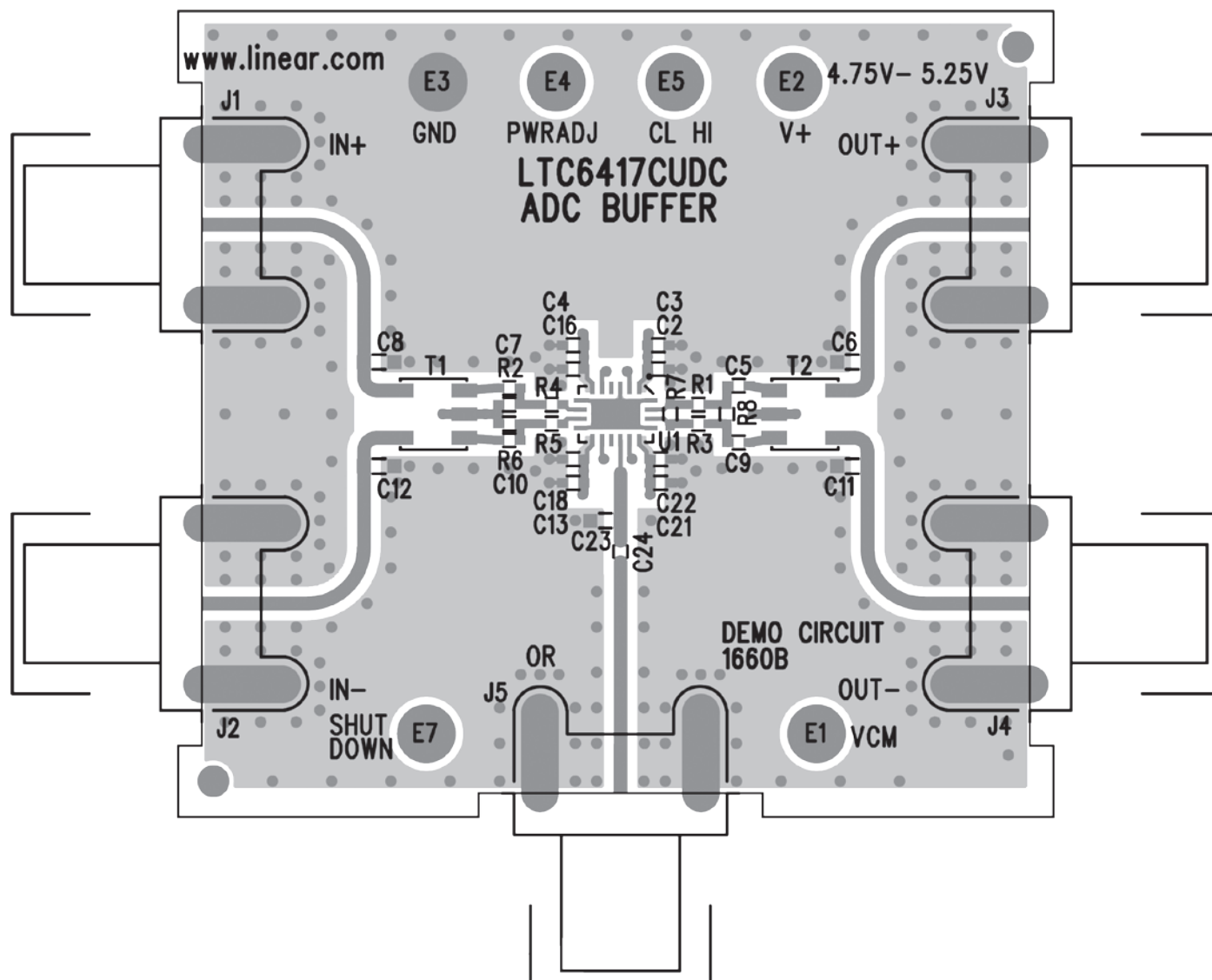


Figure 16. Demo Board DC1660B Layout

APPLICATIONS INFORMATION

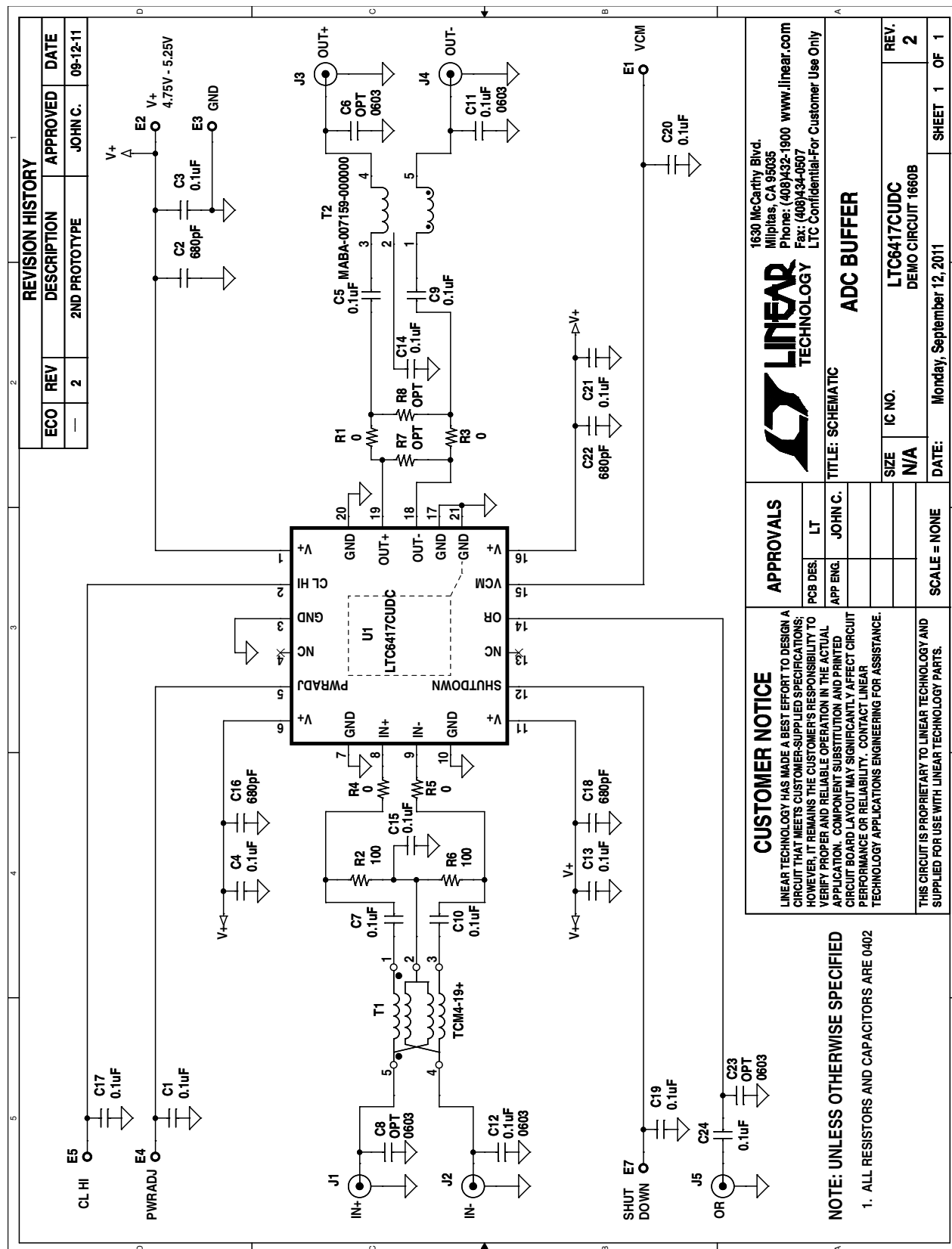


Figure 17. Demo Board DC1660B Schematic (Test Circuit A)

APPLICATIONS INFORMATION

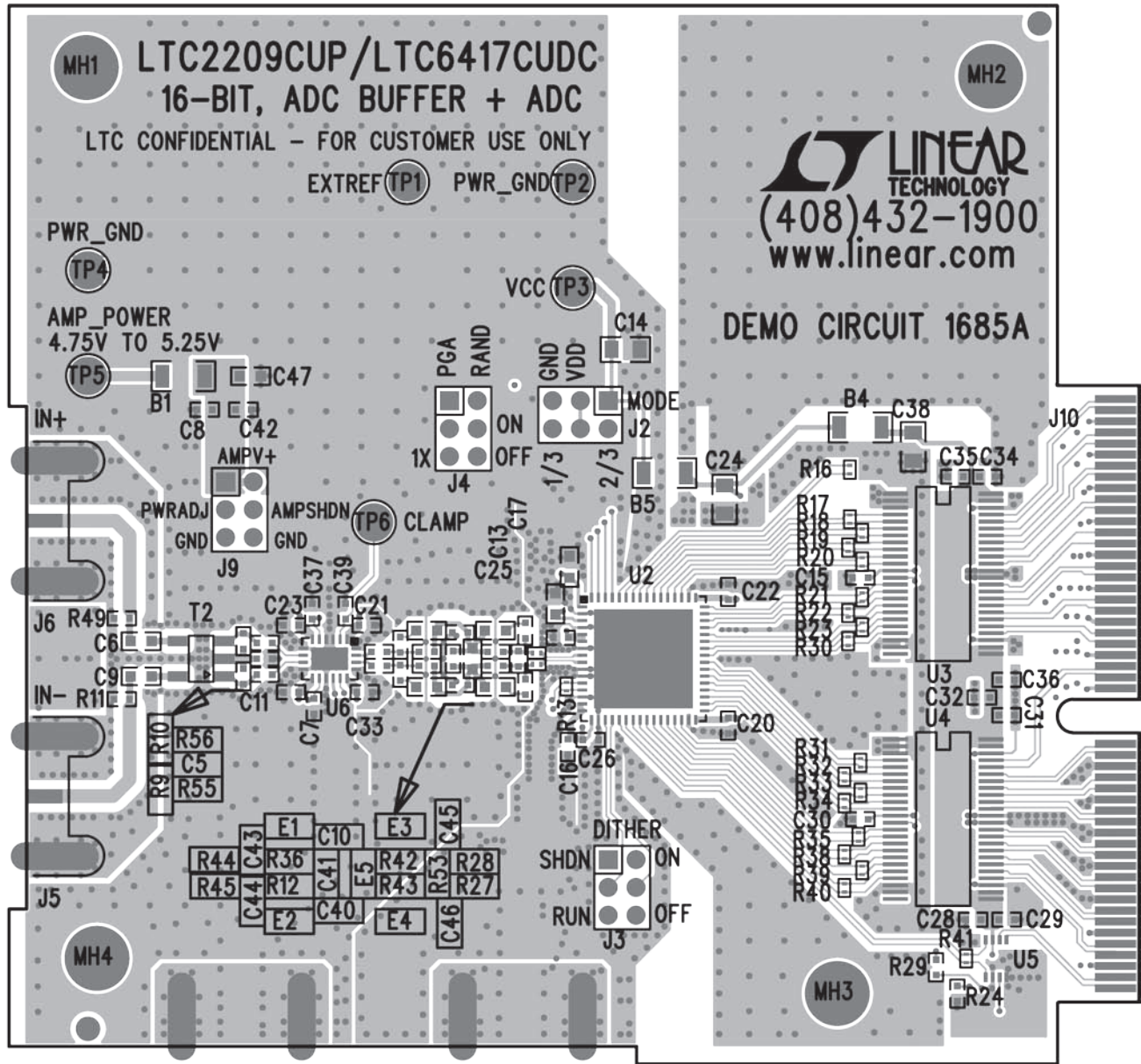


Figure 18. Demo Board DC1685A Layout

APPLICATIONS INFORMATION

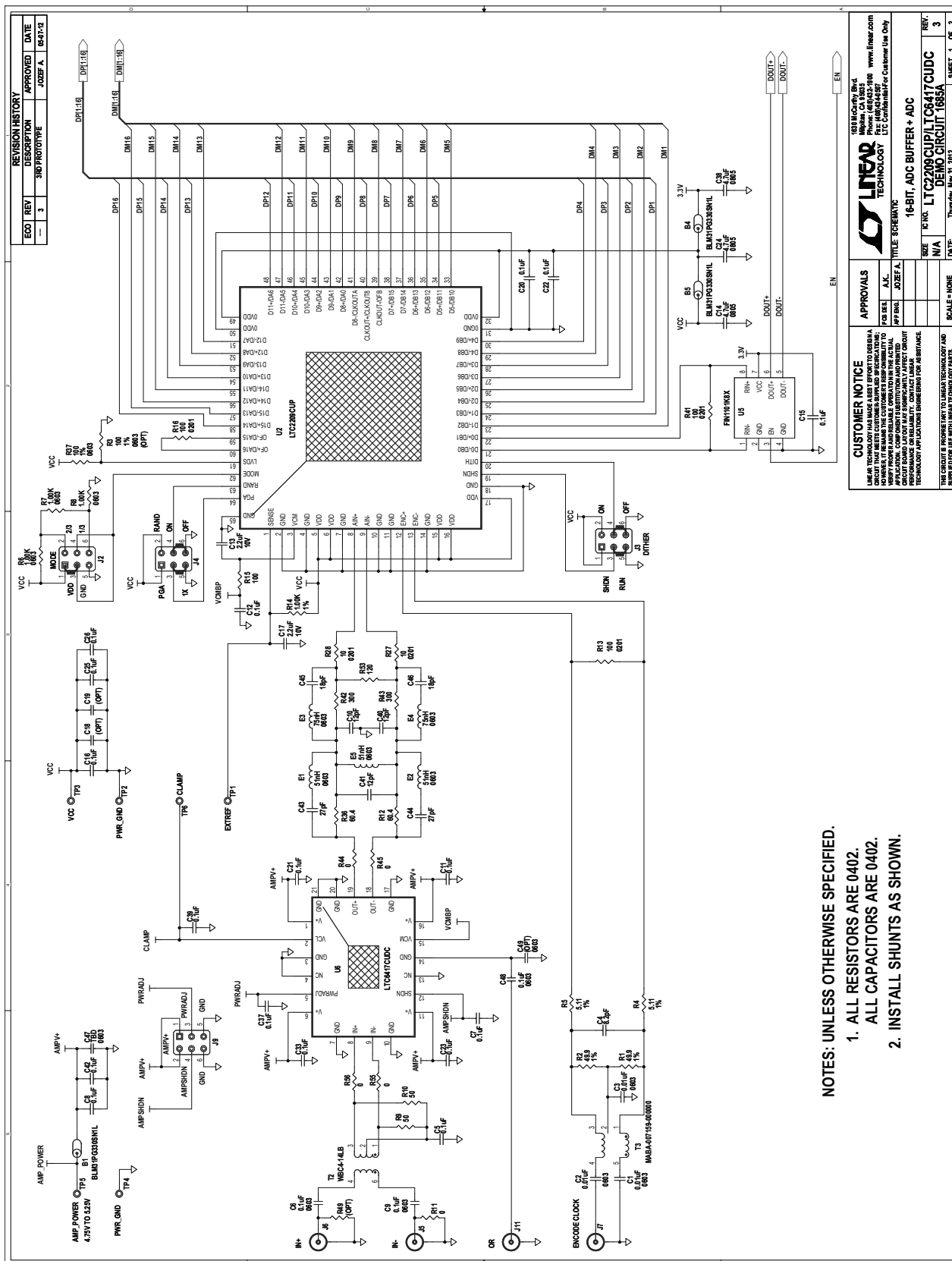
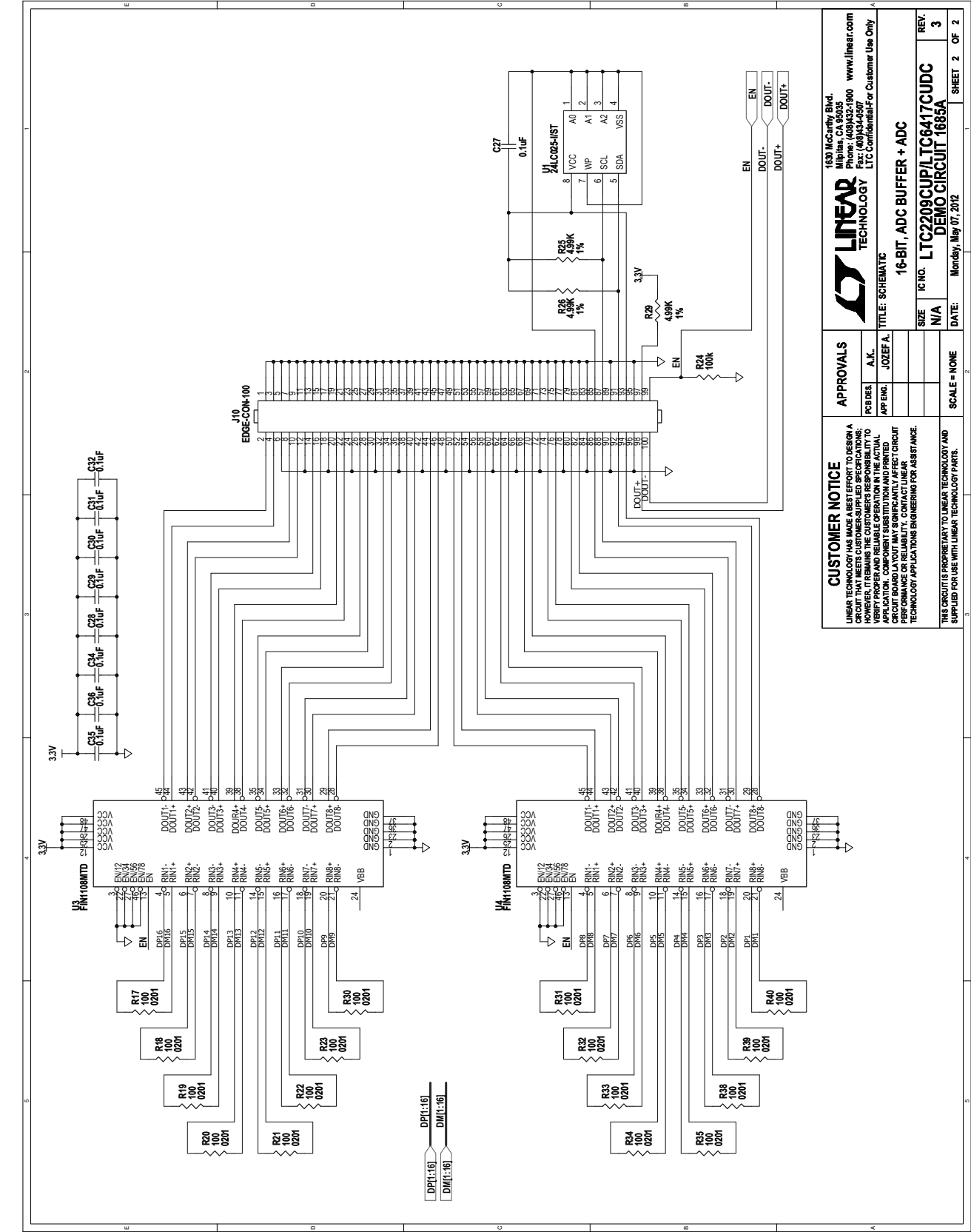


Figure 19. Demo Board DC1685A Schematic (Test Circuit B)

APPLICATIONS INFORMATION



CUSTOMER NOTICE

LINEAR TECHNOLOGY HAS MADE A BEST EFFORT TO DESIGN A SCHEMATIC FOR THE DEMO BOARD. HOWEVER, IT REMAINS THE CUSTOMER'S RESPONSIBILITY TO VERIFY PROPER AND RELIABLE OPERATION IN THE ACTUAL APPLICATION. COMPONENT SUBSTITUTION AND PRINTED CIRCUIT BOARD MANUFACTURING VARIATIONS MAY AFFECT CIRCUIT PERFORMANCE OR RELIABILITY. CONTACT LINEAR TECHNOLOGY APPLICATIONS ENGINEERING FOR ASSISTANCE.

APPROVALS

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16-BIT, ADC BUFFER + ADC

IC NO. LTC2209CJPLTC6417CUDC
DEMO CIRCUIT 1685A

SIZE	N/A
DATE	Monday, May 07, 2012

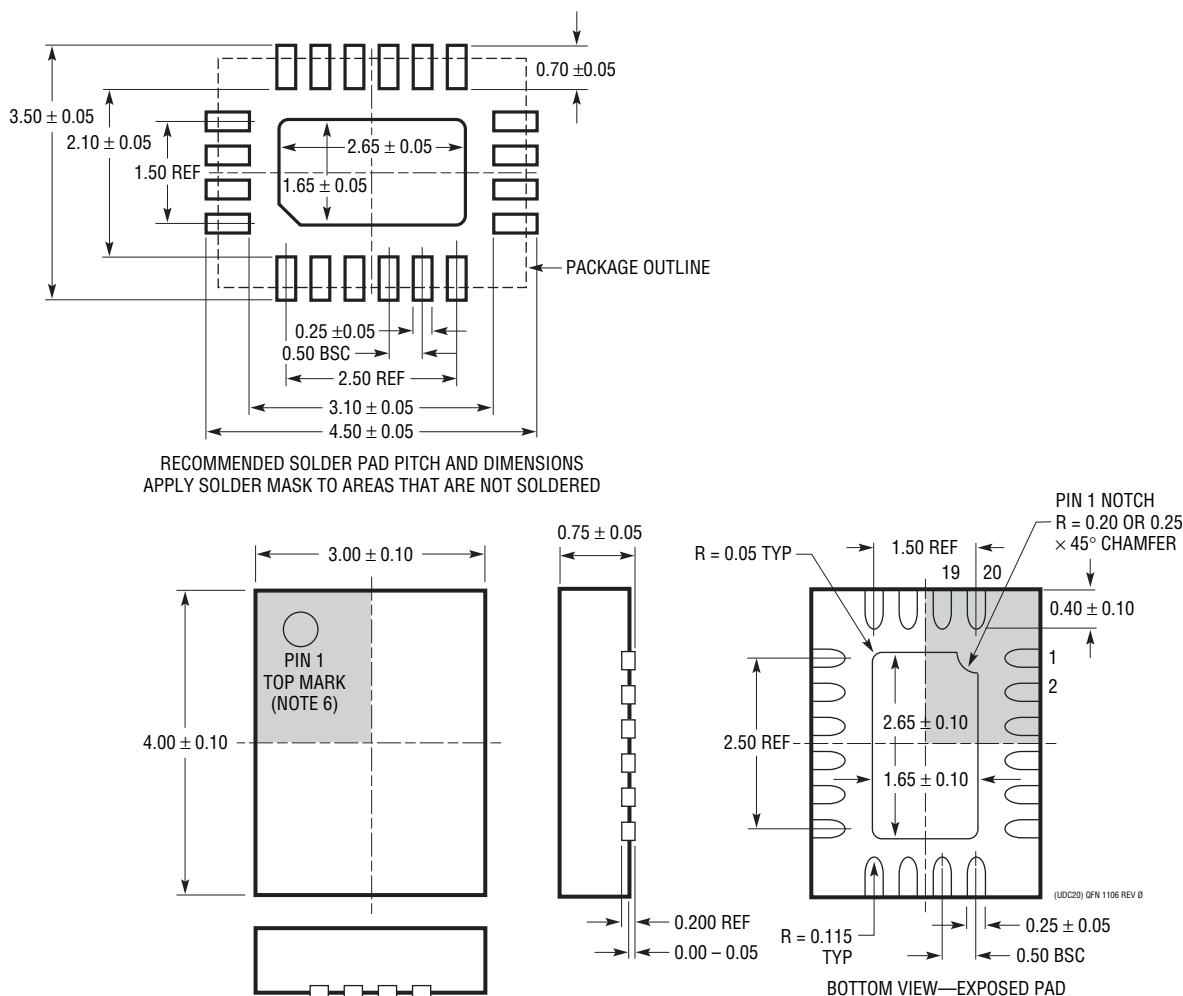
SCALE	NONE
SHEET	2 OF 2

Figure 19 (Continued). Demo Board DC1685A Schematic (Test Circuit B)

PACKAGE DESCRIPTION

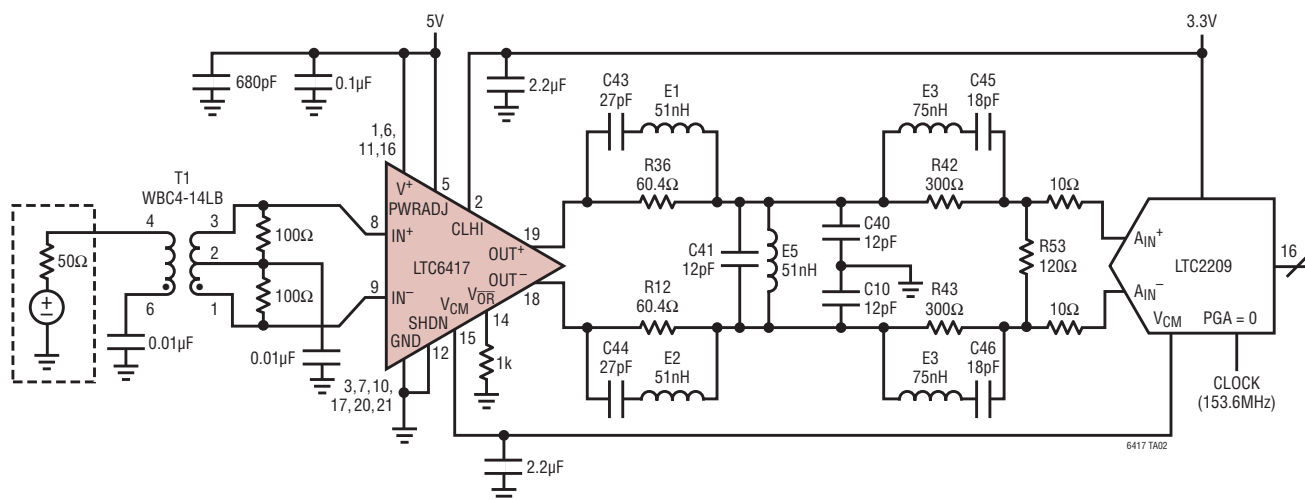
Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

UDC Package
20-Lead Plastic QFN (3mm × 4mm)
 (Reference LTC DWG # 05-08-1742 Rev 0)



TYPICAL APPLICATION

DC1685A Simplified Schematic with Suggested Output Termination for Driving an LTC2209 16-Bit ADC at 140MHz



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
Fixed Gain IF Amplifiers/ADC Drivers		
LTC6400-8/LTC6400-14/LTC6400-20/LTC6400-26	1.8GHz Low Noise, Low Distortion Differential ADC Drivers	-71dBc IM3 at 240MHz 2V _{p-p} Composite, I _S = 90mA, A _V = 8dB, 14dB, 20dB, 26dB
LTC6420-20	Dual 1.8GHz Low Noise, Low Distortion Differential ADC Drivers	Dual Version of the LTC6400-20, A _V = 8dB, 14dB, 20dB, 26dB
LTC6401-8/LTC6401-14/LTC6401-20/LTC6401-26	1.3GHz Low Noise, Low Distortion Differential ADC Drivers	-74dBc IM3 at 140MHz 2V _{p-p} Composite, I _S = 50mA, A _V = 8dB, 14dB, 20dB, 26dB
LTC6421-20	Dual 1.3GHz Low Noise, Low Distortion Differential ADC Drivers	Dual Version of the LTC6401-20, A _V = 8dB, 14dB, 20dB, 26dB
IF Amplifiers/ADC Drivers with Variable Gain		
LTC6412	800MHz, 31dB Range Analog-Controlled VGA	Continuously Adjustable Gain Control, -14dB to 17dB Linear-in-dB Gain Range
LT5554	High Dynamic Range 7-Bit Digitally Controlled IF VGA/ADC Driver	OIP3 = 46dBm at 200MHz, Gain Range 1.725 to 17.6dB 0.125dB Steps
LT5514	Ultra-Low Distortion IF Amplifier/ADC Driver with Digitally Controlled Gain	OIP3 = 47dBm at 100MHz, Gain Range 10.5dB to 33dB 1.5dB Steps
LT5524	Low Distortion IF Amplifier/ADC Driver with Digitally Controlled Gain	OIP3 = 40dBm at 100MHz, Gain Range 4.5dB to 37dB 1.5dB Steps
Baseband Differential Amplifiers		
LT6416	2GHz Low Noise Differential 16-Bit ADC Buffer	-84dBc IM3 at 160MHz 2V _{p-p} Composite, A _V = 1, e _n = 1.8nV/√Hz, 42mA
LTC6409	10GHz 1.1nV/√Hz ADC Driver	AC- or DC-Coupled 0MHz to 100MHz
LTC6406	3GHz Rail-to-Rail Input Differential Amplifier/ADC Driver	-65dBc IM3 at 50MHz 2V _{p-p} Composite, Rail-to-Rail Inputs, e _n = 1.6nV/√Hz, 18mA
LTC6404-1/LTC6404-2/LTC6404-4	Low Noise Rail-to-Rail Output Differential Amplifier/ADC Driver	16-Bit SNR and SFDR at 10MHz, Rail-to-Rail Outputs, e _n = 1.5nV/√Hz, LTC6404-1 is Unity-Gain Stable, LTC6404-2 is Gain-of-2 Stable
LTC6403-1	Low Noise Rail-to-Rail Output Differential Amplifier/ADC Driver	16-Bit SNR and SFDR at 3MHz, Rail-to-Rail Outputs, e _n = 2.8nV/√Hz
ADCs		
LTC2209	16-Bit 160Msps ADC	77.3dBFS Noise Floor, 100dB SFDR
LTC2208	16-Bit 130Msps ADC	78dBFS Noise Floor, 100dB SFDR

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