

Automotive-grade N-channel 40 V, 6.1 mΩ typ., 18 A STripFET™ F5 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

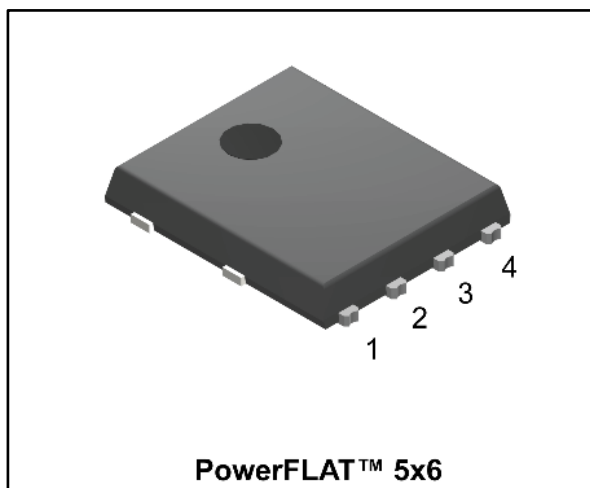
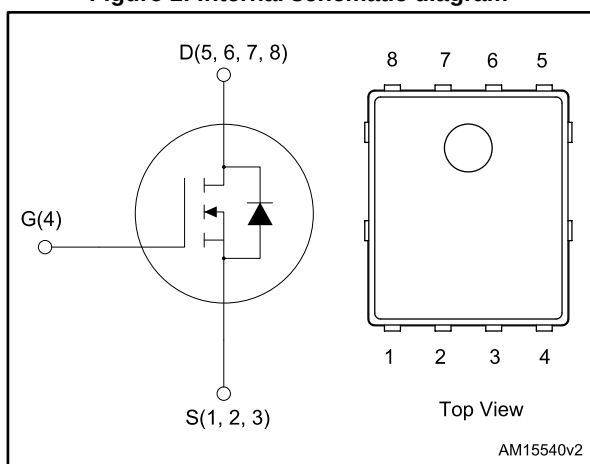


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STL70N4LLF5	40 V	6.7 mΩ	18 A

- AEC-Q101 qualified
- Low on-resistance R_{DS(on)}
- High avalanche ruggedness
- Low gate drive power loss
- Wetable flank package



Applications

- Switching applications

Description

This N-channel Power MOSFET is developed using the STripFET™ F5 technology and has been optimized to achieve very low on-state resistance, contributing to a FoM that is among the best in its class.

Table 1: Device summary

Order code	Marking	Package	Packing
STL70N4LLF5	70N4LLF5	PowerFLAT™ 5x6	Tape and reel

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
	2.2 Electrical characteristics (curves).....	6
3	Test circuits	8
4	Package information	9
	4.1 PowerFLAT™ 5x6 single island WF type C package information ..	10
	4.2 Packing information.....	13
5	Revision history	15

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	± 22	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	70	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	44	
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	18	
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$	11.5	
$I_{DM}^{(1)(3)}$	Drain current (pulsed)	72	
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	72	W
$P_{TOT}^{(2)}$	Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	4.8	
T_{stg}	Storage temperature range	-55 to 175	$^\circ\text{C}$
T_J	Operation junction temperature range		

Notes:(1)The value is rated according to R_{thj-c} .(2)The value is rated according to $R_{thj-pcb}$.

(3)Pulse width limited by safe operating area

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.08	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	31.3	

Notes:(1)When mounted on FR-4 board of 1 inch², 2oz Cu, $t < 10\text{ s}$

Table 4: Avalanche data

Symbol	Parameter	Value	Unit
I_{AV}	Not-repetitive avalanche current (pulse width limited by $T_{jmax.}$)	9	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AV}$, $V_{DD} = 24\text{ V}$)	470	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5: On/off-states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 250 µA, V _{GS} = 0 V	40			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V V _{DS} = 40 V			1	µA
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V V _{DS} = 40 V, T _J = 125 °C ⁽¹⁾			10	
I _{GSS}	Gate-body leakage current	V _{GS} = ± 22 V, V _{DS} = 0 V			±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 µA	1		2.5	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 9 A		6.1	6.7	mΩ
		V _{GS} = 4.5 V, I _D = 9 A		7.6	9.0	

Notes:

⁽¹⁾Defined by design, not subject to production test

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0 V	-	1570	-	pF
C _{oss}	Output capacitance		-	257	-	pF
C _{rss}	Reverse transfer capacitance		-	32	-	pF
Q _g	Total gate charge	V _{DD} = 15 V, I _D = 18 A, V _{GS} = 4.5 V (see Figure 14: "Test circuit for gate charge behavior")	-	12.9	-	nC
Q _{gs}	Gate-source charge		-	3.9	-	nC
Q _{gd}	Gate-drain charge		-	5.3	-	nC
R _G	Gate input resistance	f = 1 MHz, gate DC bias = 0 V, test signal level = 20 mV, I _D = 0 A	-	1.5	-	Ω

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 15 V, I _D = 9 A, R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 13: "Test circuit for resistive load switching times")	-	14	-	ns
t _r	Rise time		-	42	-	ns
t _{d(off)}	Turn-off delay time		-	37	-	ns
t _f	Fall time		-	5.2	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		18	A
$I_{SDM}^{(1)}$	Source-drain current pulsed		-		72	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 18\text{ A}$, $V_{GS} = 0\text{ V}$			1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 18\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 25\text{ V}$, $T_J = 150\text{ }^{\circ}\text{C}$	-	27.2		ns
Q_{rr}	Reverse recovery charge		-	24.5		nC
I_{RRM}	Reverse recovery current		-	1.8		A

Notes:

⁽¹⁾Pulse width limited by safe operating area.

⁽²⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.2 Electrical characteristics (curves)

Figure 2: Safe operating area

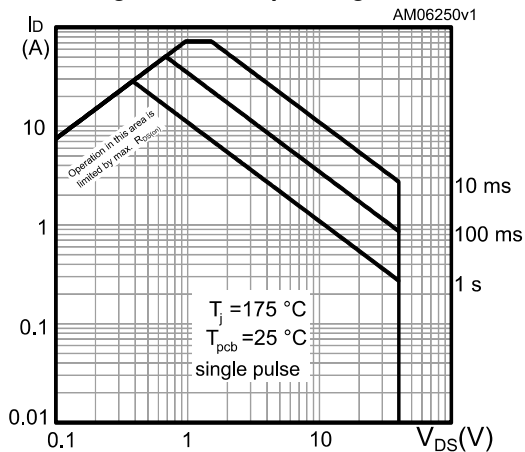


Figure 3: Thermal impedance

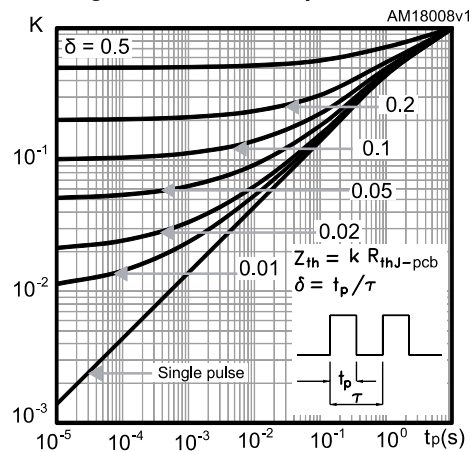


Figure 4: Output characteristics

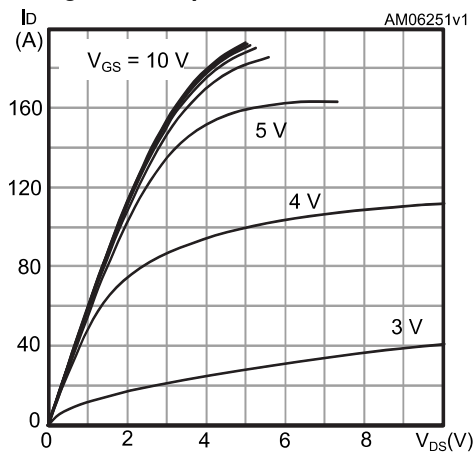


Figure 5: Transfer characteristics

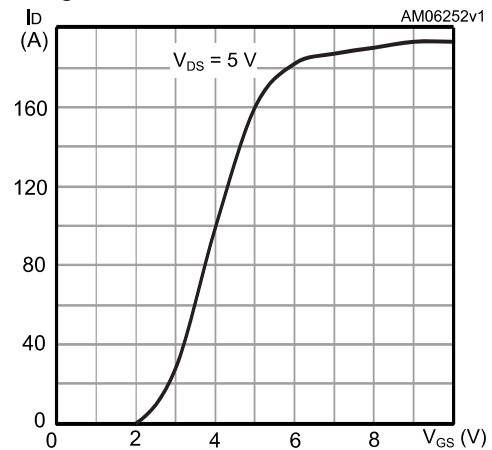
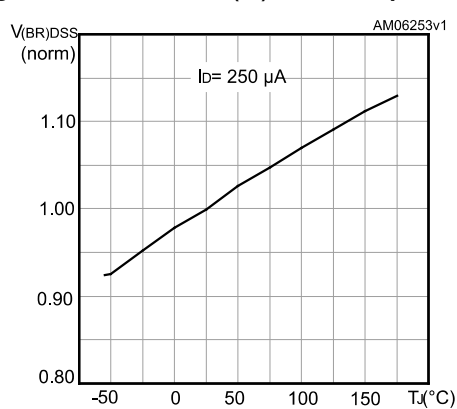
Figure 6: Normalized $V_{(BR)DSS}$ vs. temperature

Figure 7: Static drain-source on-resistance

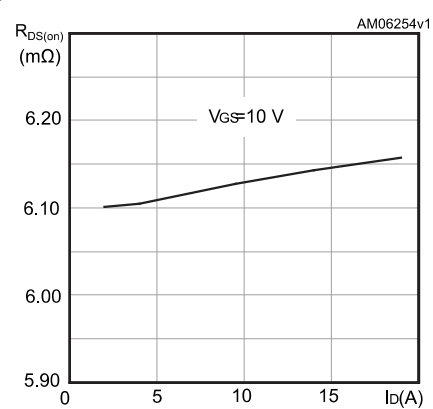


Figure 8: Gate charge vs. gate-source voltage

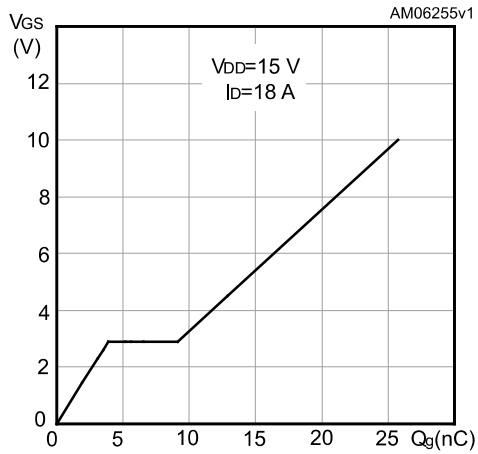


Figure 9: Capacitance variations

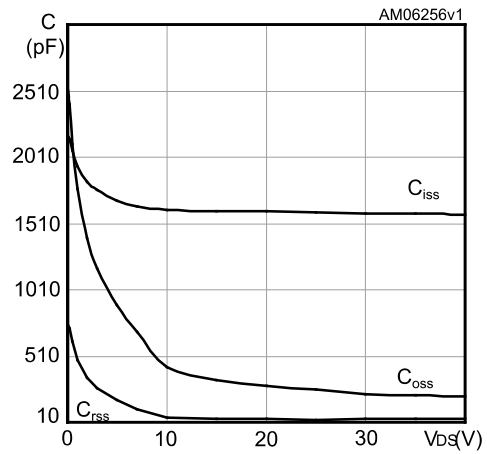


Figure 10: Normalized gate threshold voltage vs. temperature

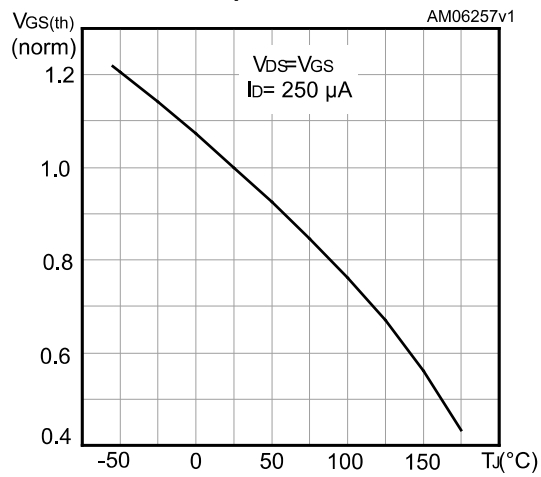


Figure 11: Normalized on-resistance vs. temperature

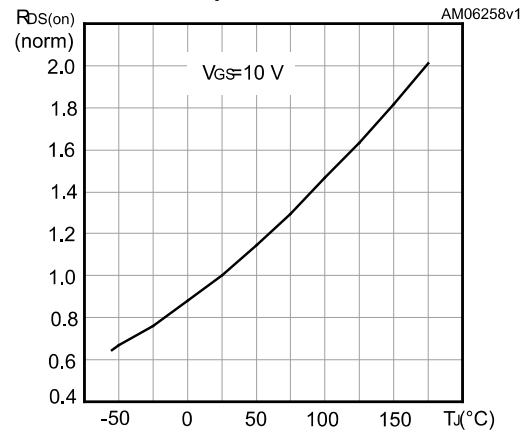
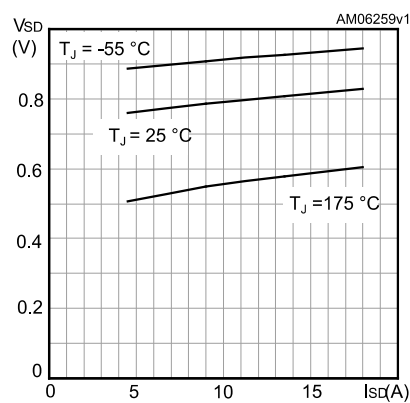


Figure 12: Source-drain diode forward characteristics



3 Test circuits

Figure 13: Test circuit for resistive load switching times



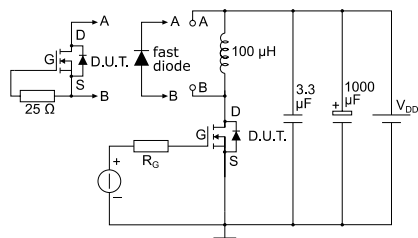
AM01468v1

Figure 14: Test circuit for gate charge behavior



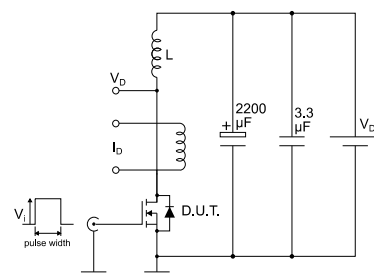
AM01469v1

Figure 15: Test circuit for inductive load switching and diode recovery times



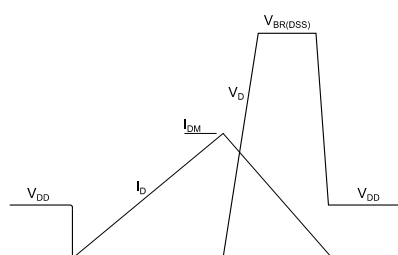
AM01470v1

Figure 16: Unclamped inductive load test circuit



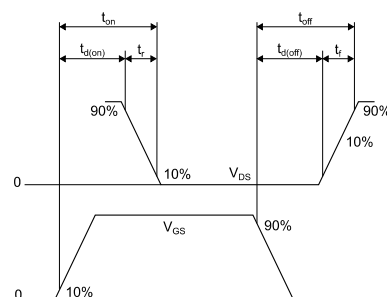
AM01471v1

Figure 17: Unclamped inductive waveform



AM01472v1

Figure 18: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 5x6 single island WF type C package information

Figure 19: PowerFLAT™ 5x6 WF type C package outline

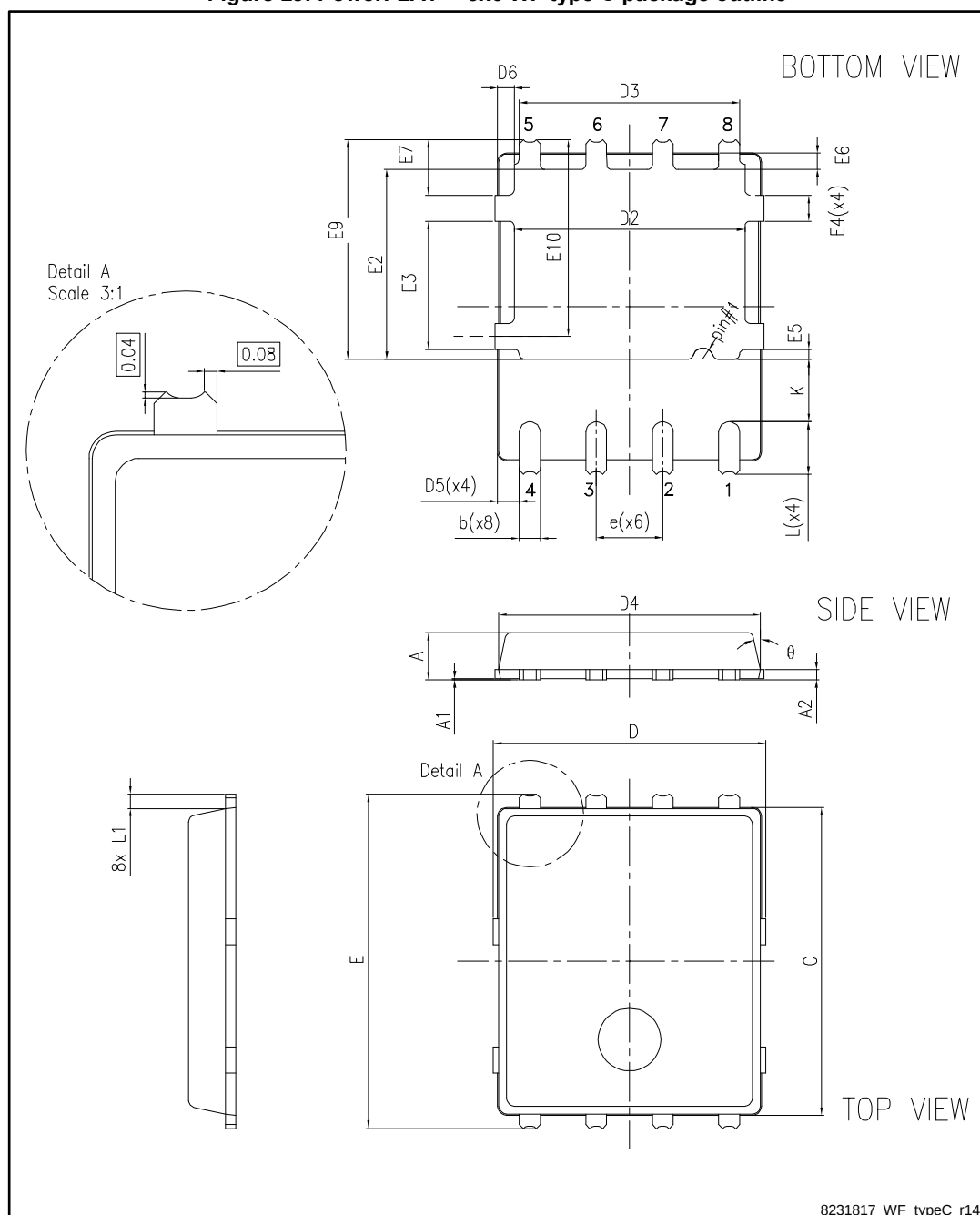
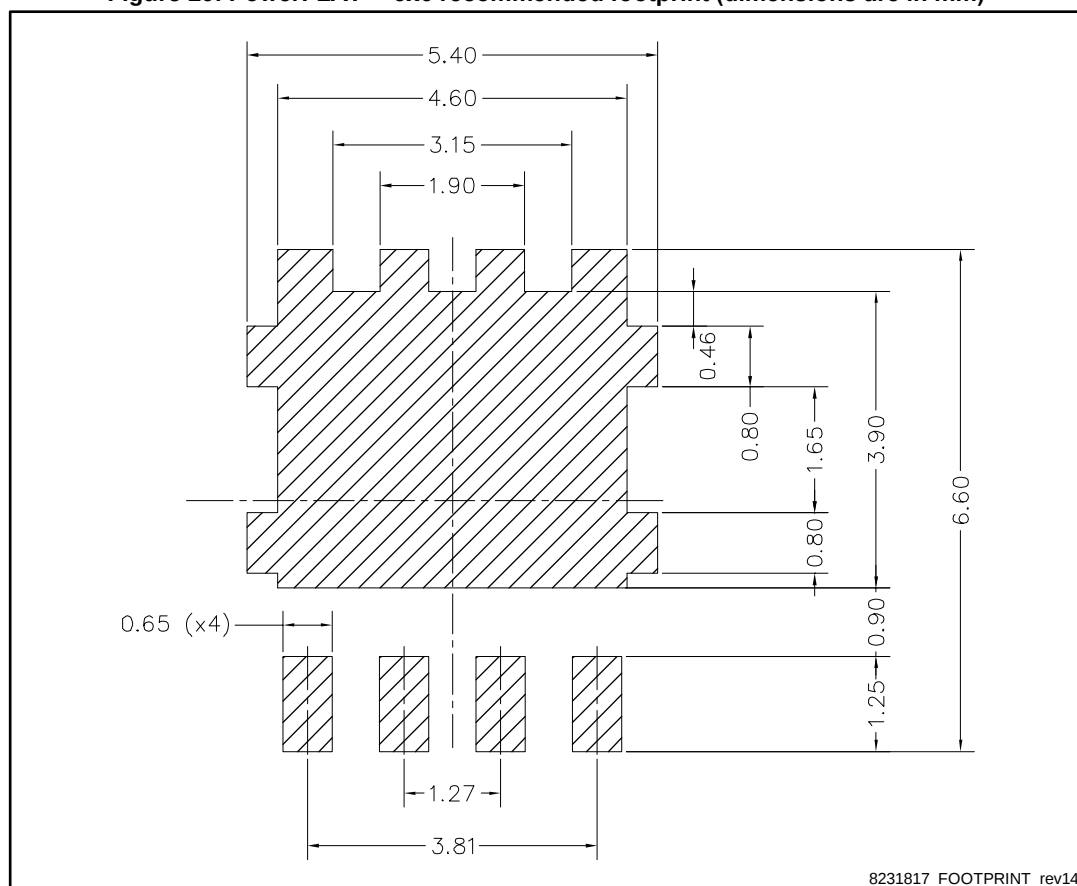


Table 9: PowerFLAT™ 5x6 WF type C mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.10
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.10
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
e		1.27	
E	6.20	6.40	6.60
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.85	1.00	1.15
E9	4.00	4.20	4.40
E10	3.55	3.70	3.85
K	1.05		1.35
L	0.90	1.00	1.10
L1	0.175	0.275	0.375
θ	0°		12°

Figure 20: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



4.2 Packing information

Figure 21: PowerFLAT™ 5x6 WF tape (dimensions are in mm)

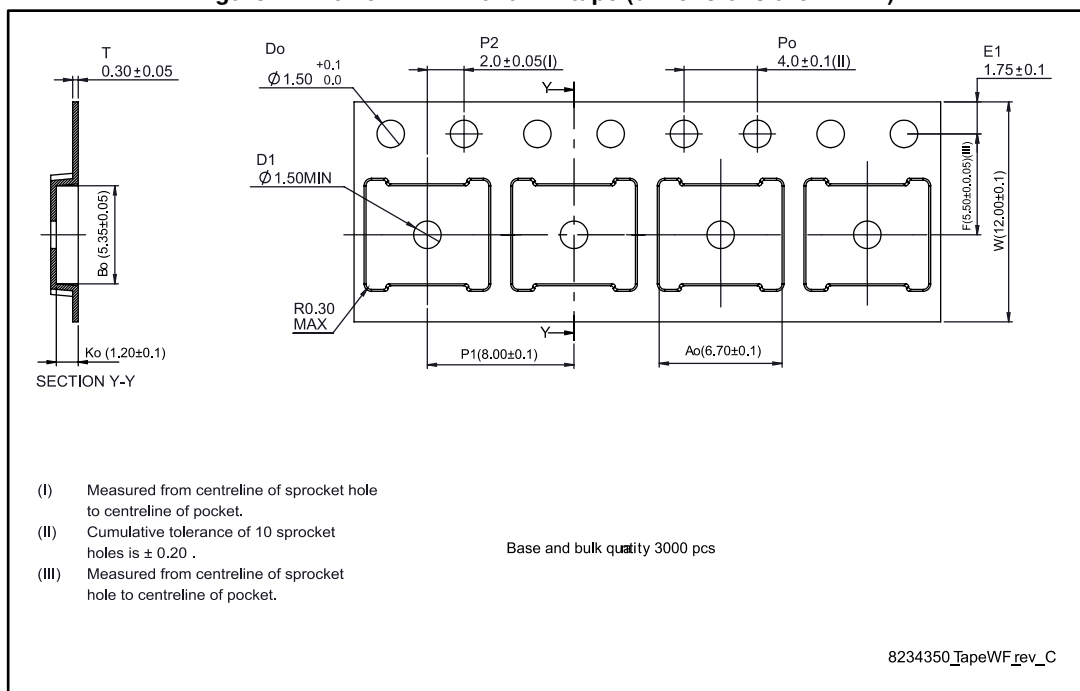


Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape

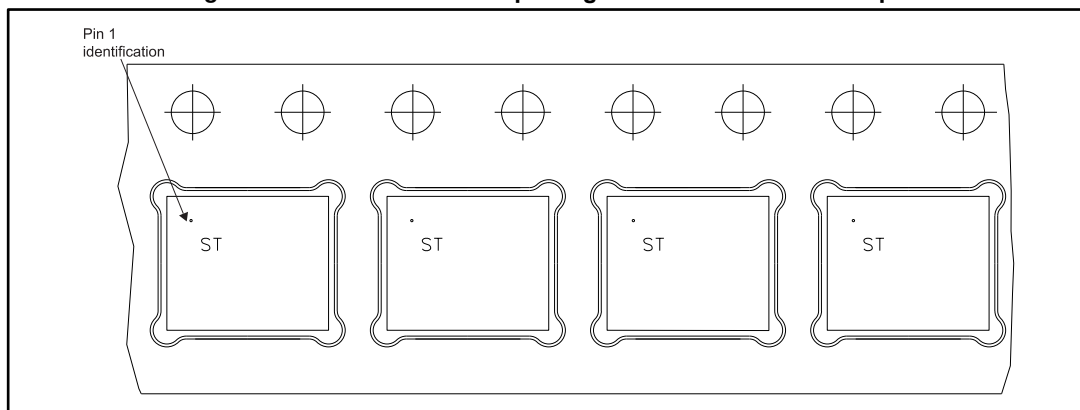
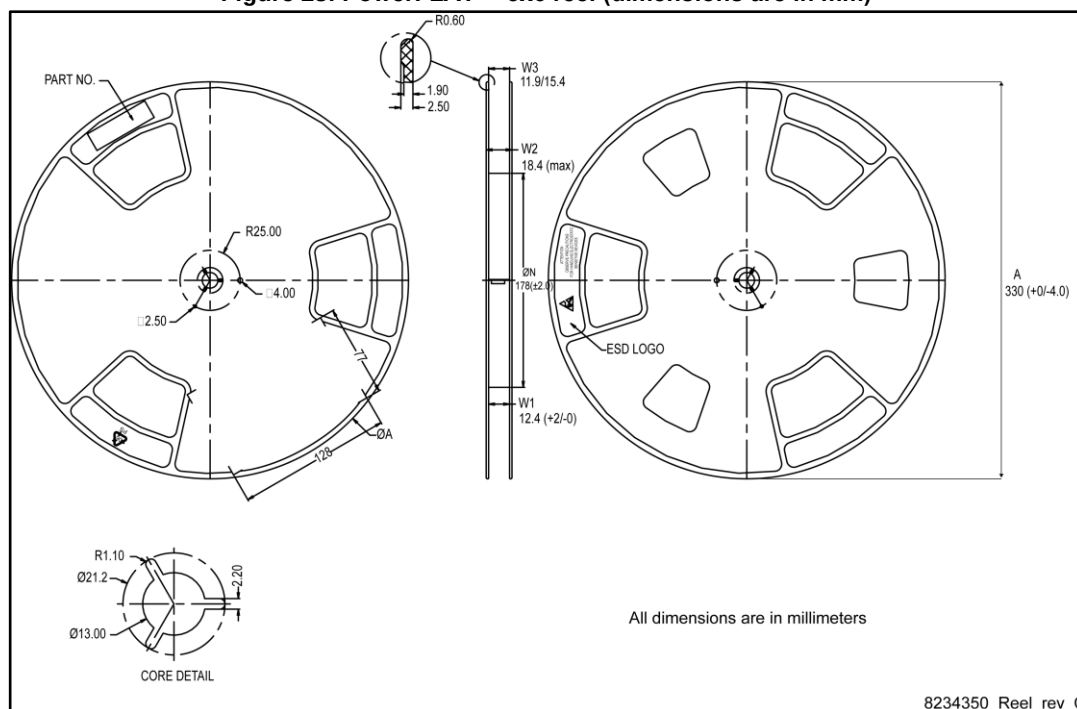


Figure 23: PowerFLAT™ 5x6 reel (dimensions are in mm)



5 Revision history

Table 10: Document revision history

Date	Revision	Changes
01-Dec-2008	1	First release.
18-Jul-2011	2	Section 4: Package mechanical data has been modified: – Added <i>Table 9: PowerFLAT™ 5x6 type S-C mechanical data</i> – Added <i>Figure 19: PowerFLAT™ 5x6 type S-C mechanical data</i> – Added <i>PowerFLAT™ 5x6 type C-B mechanical data</i> – Added <i>PowerFLAT™ 5x6 type C-B drawing</i> Minor text changes.
21-Dec-2011	3	Section 4: Package mechanical data has been modified.
25-Jan-2013	4	– Table 1: Device summary has been updated. -Minor text changes. –Changed: <i>Figure 1</i> -Added <i>Section 5: Packaging mechanical data</i> .
12-Feb-2013	5	-Updated T_J and T_{stg} in Table 2: Absolute maximum ratings. – Updated <i>Section 4: Package mechanical data</i> and <i>Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape</i> .
24-May-2013	6	– Modified: title and <i>Section 4: Package mechanical data</i> - Minor text changes.
17-Dec-2014	7	– Modified: Figure 2 and 3 – Updated: Figure 13, 14, 15 and 16 – Updated: Section 4: Package mechanical data and Section 5: Packaging mechanical data – Minor text changes.
08-Apr-2016	8	– Updated <i>Section 4: Package information</i> and <i>Section 4.1: Packing information</i> -Minor text changes.
22-Sep-2016	9	Updated $V_{GS(th)}$ in <i>Table 5: "On/off-states"</i> .

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2016 STMicroelectronics – All rights reserved