

FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Military temperature range (-55°C to $+125^{\circ}\text{C}$)
- Controlled manufacturing baseline
- One assembly/test site
- One fabrication site
- Enhanced product change notification
- Qualification data available on request
- Wide bandwidth: 15 MHz
- Low offset voltage: 325 μV maximum
- Low noise: 9.5 nV/ $\sqrt{\text{Hz}}$ @ 1 kHz
- Single-supply operation: 2.7 V to 12 V
- Low supply current: 850 μA maximum
- Rail-to-rail output swing
- Low TCV_{OS} : 1 $\mu\text{V}/^{\circ}\text{C}$ typical
- High slew rate: 13 V/ μs
- No phase inversion
- Unity-gain stable

APPLICATIONS

- Portable instrumentation
- Sampling ADC amplifiers
- Precision filters

PIN CONFIGURATION

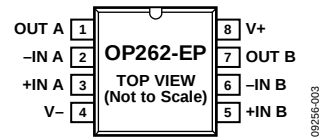


Figure 1. 8-Lead Narrow-Body SOIC (R Suffix)

GENERAL DESCRIPTION

The OP262-EP is a low power, precision op amp that features a rail-to-rail output and a 15 MHz bandwidth. With its low offset voltage of 45 μV (typical) and low noise, it is well suited for precision filter and control applications.

This product operates from a single supply as low as 2.7 V or from dual supplies up to ± 6 V. The OP262-EP is specified over the military temperature range (-55°C to $+125^{\circ}\text{C}$) and is available in an 8-lead SOIC_N package.

Additional applications information is available in the [OP162/OP262/OP462](#) data sheet.

Rev. 0

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REVISION HISTORY

7/10—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

$V_S = 5.0\text{ V}$, $V_{CM} = 0\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		45	325	μV
Input Bias Current	I_B	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		360	600	nA
Input Offset Current	I_{OS}	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		± 2.5	± 25	nA
Input Voltage Range	V_{CM}	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	0		4	V
Common-Mode Rejection	CMRR	$0\text{ V} \leq V_{CM} \leq 4.0\text{ V}$, $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	70	110		dB
Large Signal Voltage Gain	A_{VO}	$R_L = 2\text{ k}\Omega$, $0.5 \leq V_{OUT} \leq 4.5\text{ V}$		30		V/mV
		$R_L = 10\text{ k}\Omega$, $0.5 \leq V_{OUT} \leq 4.5\text{ V}$	65	88		V/mV
		$R_L = 10\text{ k}\Omega$, $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	40			V/mV
Offset Voltage Drift ¹	$\Delta V_{OS}/\Delta T$			1		$\mu\text{V}/^\circ\text{C}$
Bias Current Drift	$\Delta I_B/\Delta T$			250		pA/ $^\circ\text{C}$
OUTPUT CHARACTERISTICS						
Output Voltage Swing High	V_{OH}	$I_L = 250\text{ }\mu\text{A}$, $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	4.95	4.99		V
		$I_L = 5\text{ mA}$	4.85	4.94		V
Output Voltage Swing Low	V_{OL}	$I_L = 250\text{ }\mu\text{A}$, $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		14	50	mV
		$I_L = 5\text{ mA}$		65	150	mV
Short-Circuit Current	I_{SC}	Short to ground		± 80		mA
Maximum Output Current	I_{OUT}			± 30		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = 2.7\text{ V}$ to 7 V $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	90	120		dB
Supply Current/Amplifier	I_{SY}	$V_{OUT} = 2.5\text{ V}$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		500	700	μA
					850	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$1\text{ V} < V_{OUT} < 4\text{ V}$, $R_L = 10\text{ k}\Omega$		10		V/ μs
Settling Time	t_s	To 0.1%, $A_V = -1$, $V_O = 2\text{ V}$ step		540		ns
Gain Bandwidth Product	GBP			15		MHz
Phase Margin	ϕ_m			61		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.5		$\mu\text{V p-p}$
Voltage Noise Density	e_n	$f = 1\text{ kHz}$		9.5		nV/ $\sqrt{\text{Hz}}$
Current Noise Density	i_n	$f = 1\text{ kHz}$		0.4		pA/ $\sqrt{\text{Hz}}$

¹ Offset voltage drift is the average of the -55°C to $+25^\circ\text{C}$ delta and the $+25^\circ\text{C}$ to $+125^\circ\text{C}$ delta.

OP262-EP

$V_S = 3.0\text{ V}$, $V_{CM} = 0\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V _{OS}	−55°C ≤ T _A ≤ +125°C		50	325	μV
Input Bias Current	I _B				1	mV
Input Offset Current	I _{OS}			360	600	nA
Input Voltage Range	V _{CM}			±2.5	±25	nA
Common-Mode Rejection	CMRR			0		2
Large Signal Voltage Gain	A _{VO}	0 V ≤ V _{CM} ≤ 2.0 V, −55°C ≤ T _A ≤ +125°C	70	110		dB
		R _L = 2 kΩ, 0.5 V ≤ V _{OUT} ≤ 2.5 V		20		V/mV
		R _L = 10 kΩ, 0.5 V ≤ V _{OUT} ≤ 2.5 V	20	30		V/mV
OUTPUT CHARACTERISTICS						
Output Voltage Swing High	V _{OH}	I _L = 250 μA	2.95	2.99		V
		I _L = 5 mA	2.85	2.93		V
Output Voltage Swing Low	V _{OL}	I _L = 250 μA		14	50	mV
		I _L = 5 mA		66	150	mV
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V _S = 2.7 V to 7 V −55°C ≤ T _A ≤ +125°C	60	110		dB
Supply Current/Amplifier	I _{SY}	V _{OUT} = 1.5 V −55°C ≤ T _A ≤ +125°C		500	650	μA
					850	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R _L = 10 kΩ		10		V/μs
Settling Time	t _s	To 0.1%, A _v = −1, V _O = 2 V step		575		ns
Gain Bandwidth Product	GBP			15		MHz
Phase Margin	φ _m			59		Degrees
NOISE PERFORMANCE						
Voltage Noise	e _n p-p	0.1 Hz to 10 Hz		0.5		μV p-p
Voltage Noise Density	e _n	f = 1 kHz		9.5		nV/√Hz
Current Noise Density	i _n	f = 1 kHz		0.4		pA/√Hz

$V_S = \pm 5.0 \text{ V}$, $V_{CM} = 0 \text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		25	325	μV
Input Bias Current	I_B	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		260	500	nA
Input Offset Current	I_{OS}	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		± 2.5	± 25	nA
Input Voltage Range	V_{CM}	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	-5		± 4	V
Common-Mode Rejection	CMRR	$-4.9 \text{ V} \leq V_{CM} \leq +4.0 \text{ V}$, $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	70	110		dB
Large Signal Voltage Gain	A_{VO}	$R_L = 2 \text{ k}\Omega$, $-4.5 \text{ V} \leq V_{OUT} \leq +4.5 \text{ V}$		35		V/mV
		$R_L = 10 \text{ k}\Omega$, $-4.5 \text{ V} \leq V_{OUT} \leq +4.5 \text{ V}$	75	120		V/mV
		$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	25			V/mV
Long-Term Offset Voltage ¹	V_{OS}				600	μV
Offset Voltage Drift ²	$\Delta V_{OS}/\Delta T$			1		$\mu\text{V}/^\circ\text{C}$
Bias Current Drift	$\Delta I_B/\Delta T$			250		$\text{pA}/^\circ\text{C}$
OUTPUT CHARACTERISTICS						
Output Voltage Swing High	V_{OH}	$I_L = 250 \mu\text{A}$, $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	4.95	4.99		V
		$I_L = 5 \text{ mA}$	4.85	4.94		V
Output Voltage Swing Low	V_{OL}	$I_L = 250 \mu\text{A}$, $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		-4.99	-4.95	V
		$I_L = 5 \text{ mA}$		-4.94	-4.85	V
Short-Circuit Current	I_{SC}	Short to ground		± 80		mA
Maximum Output Current	I_{OUT}			± 30		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = \pm 1.35 \text{ V to } \pm 6 \text{ V}$		110		dB
		$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	60			dB
Supply Current/Amplifier	I_{SY}	$V_{OUT} = 0 \text{ V}$		650	800	μA
		$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			1.15	mA
		$V_{OUT} = 0 \text{ V}$		550	775	μA
		$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			1	mA
Supply Voltage Range	V_S		3.0 (± 1.5)		12 (± 6)	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	$-4 \text{ V} < V_{OUT} < +4 \text{ V}$, $R_L = 10 \text{ k}\Omega$		13		V/ μs
Settling Time	t_S	To 0.1%, $A_V = -1$, $V_O = 2 \text{ V}$ step		475		ns
Gain Bandwidth Product	GBP			15		MHz
Phase Margin	ϕ_m			64		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.5		$\mu\text{V p-p}$
Voltage Noise Density	e_n	$f = 1 \text{ kHz}$		9.5		nV/ $\sqrt{\text{Hz}}$
Current Noise Density	i_n	$f = 1 \text{ kHz}$		0.4		pA/ $\sqrt{\text{Hz}}$

¹ Long-term offset voltage is guaranteed by a 1000 hour life test performed on three independent lots at 125°C , with an LTPD of 1.3.

² Offset voltage drift is the average of the -55°C to $+25^\circ\text{C}$ delta and the $+25^\circ\text{C}$ to $+125^\circ\text{C}$ delta.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Min
Supply Voltage	$\pm 6\text{ V}$
Input Voltage ¹	$\pm 6\text{ V}$
Differential Input Voltage ²	$\pm 0.6\text{ V}$
Internal Power Dissipation SOIC (S)	Observe Derating Curves
Output Short-Circuit Duration	Observe Derating Curves
Storage Temperature Range	-65°C to $+150^{\circ}\text{C}$
Operating Temperature Range	-55°C to $+125^{\circ}\text{C}$
Junction Temperature Range	-65°C to $+150^{\circ}\text{C}$
Lead Temperature Range, (Soldering, 10 sec)	300°C

¹ For supply voltages greater than 6 V, the input voltage is limited to less than or equal to the supply voltage.

² For differential input voltages greater than 0.6 V, the input current should be limited to less than 5 mA to prevent degradation or destruction of the input devices.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 5.

Package Type	θ_{JA} ¹	θ_{JC}	Unit
8-Lead SOIC (R)	157	56	$^{\circ}\text{C}/\text{W}$

¹ θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for a device soldered in circuit board for SOIC package.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

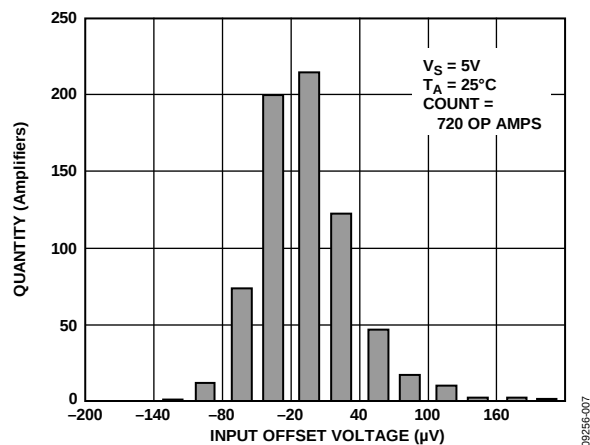


Figure 2. Input Offset Voltage Distribution

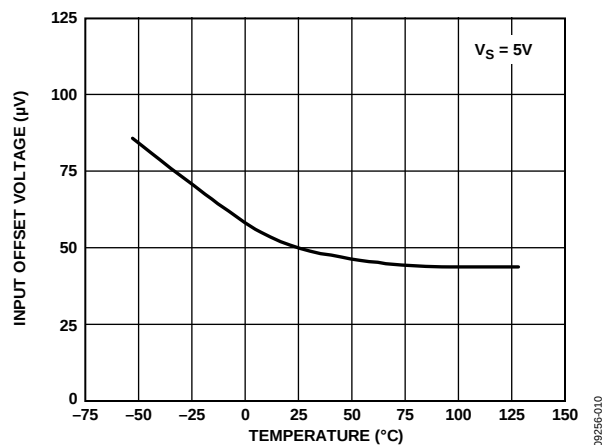


Figure 5. Input Offset Voltage vs. Temperature

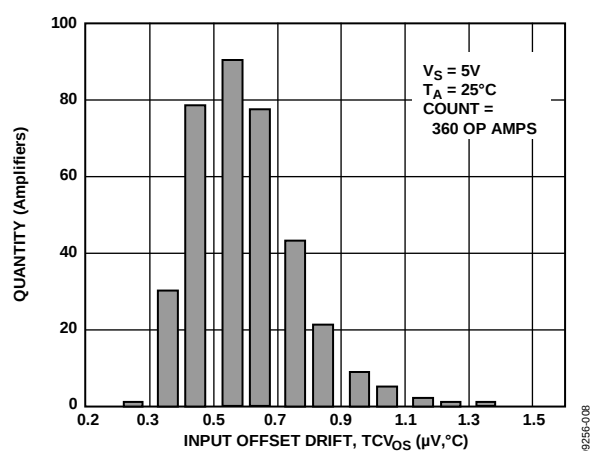


Figure 3. Input Offset Voltage Drift (TCV_{OS})

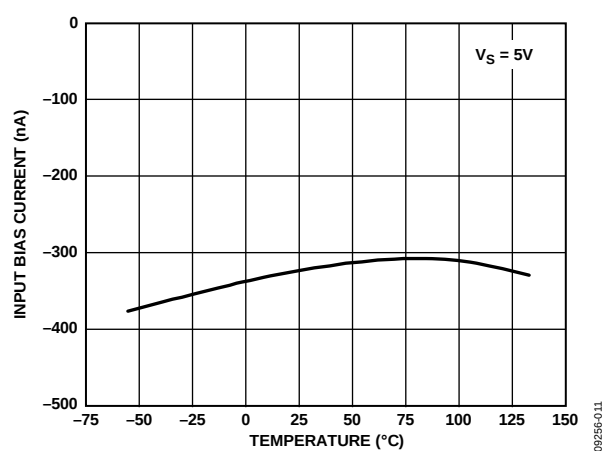


Figure 6. Input Bias Current vs. Temperature

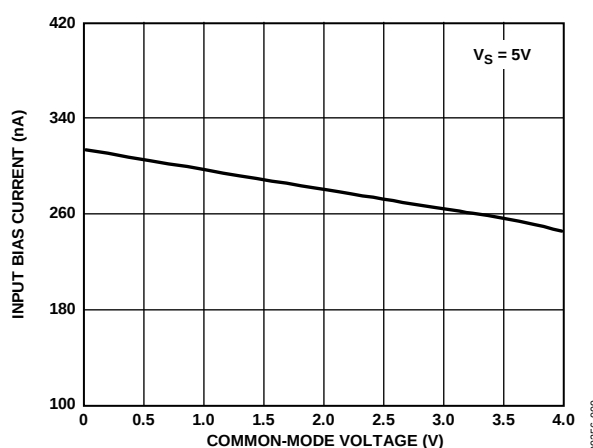


Figure 4. Input Bias Current vs. Common-Mode Voltage

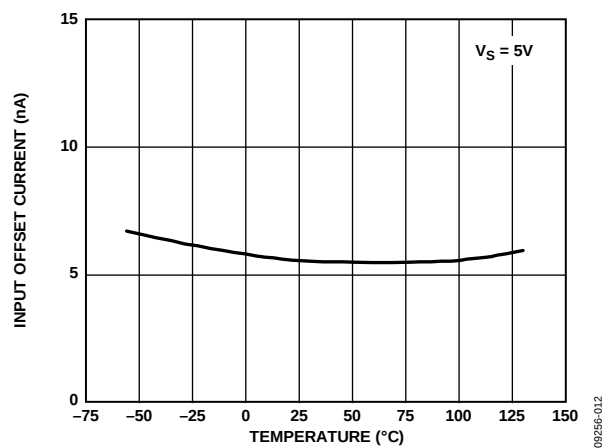


Figure 7. Input Offset Current vs. Temperature

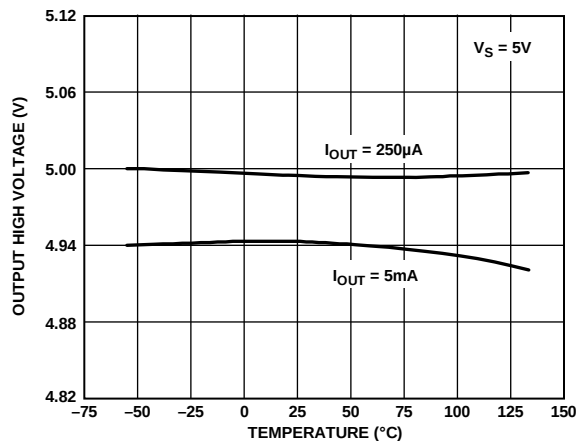


Figure 8. Output High Voltage vs. Temperature

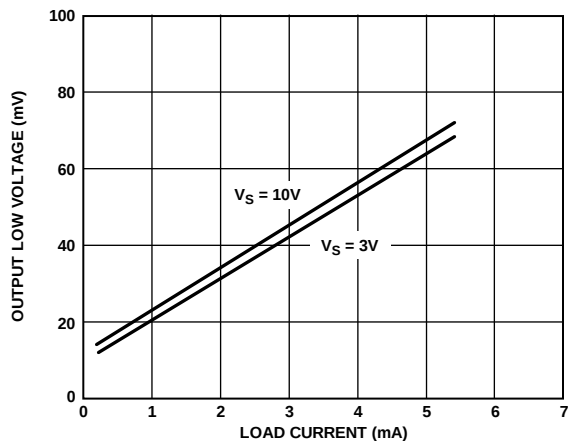


Figure 11. Output Low Voltage to Supply Rail vs. Load Current

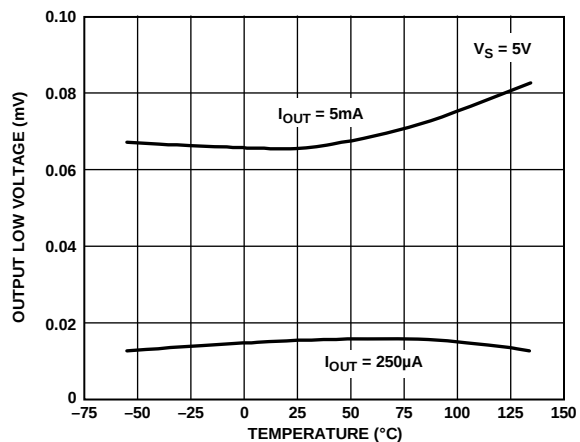


Figure 9. Output Low Voltage vs. Temperature

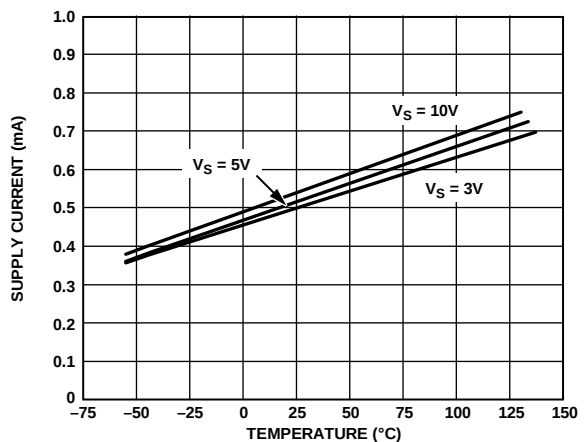


Figure 12. Supply Current/Amplifier vs. Temperature

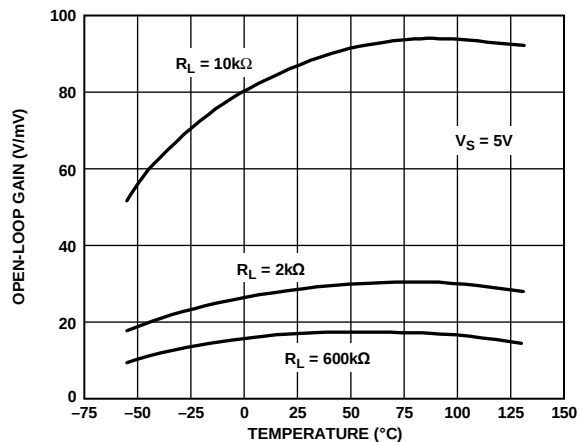


Figure 10. Open-Loop Gain vs. Temperature

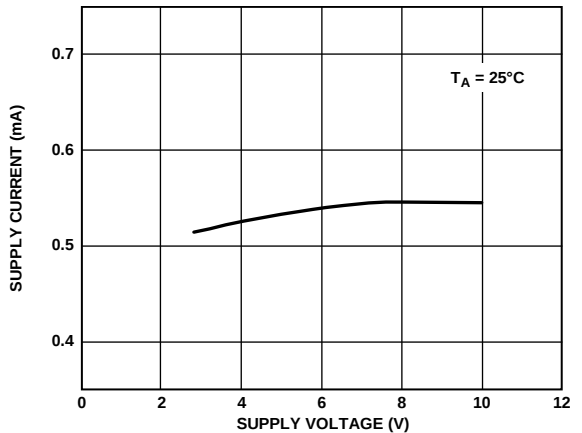


Figure 13. Supply Current/Amplifier vs. Supply Voltage

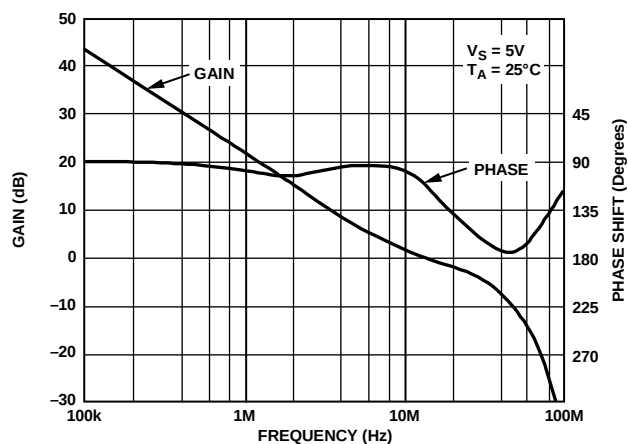


Figure 14. Open-Loop Gain and Phase vs. Frequency (No Load)

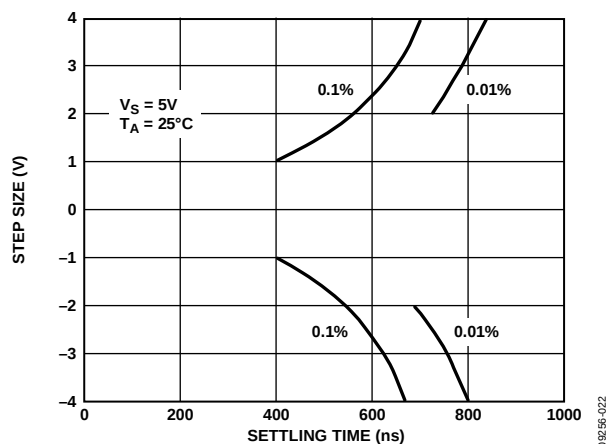


Figure 17. Step Size vs. Settling Time

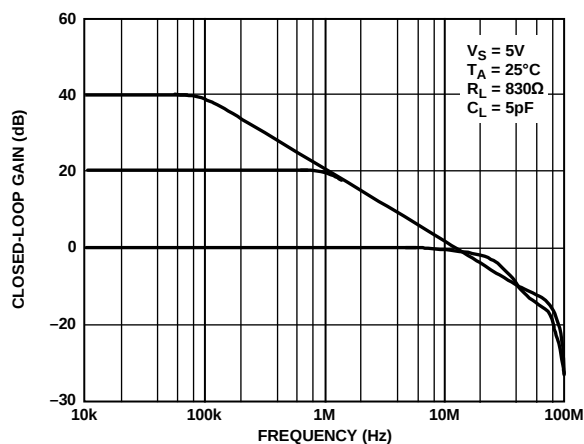


Figure 15. Closed-Loop Gain vs. Frequency

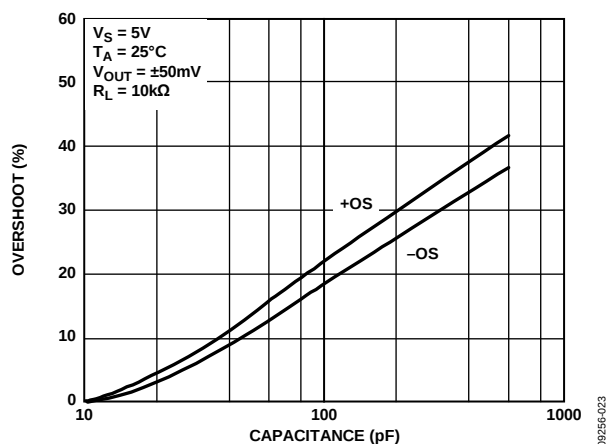


Figure 18. Small-Signal Overshoot vs. Capacitance

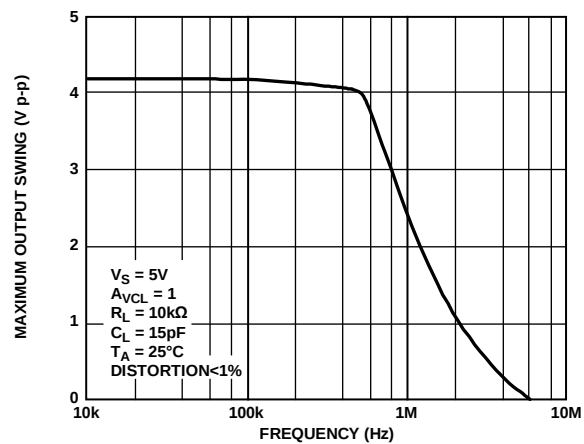


Figure 16. Maximum Output Swing vs. Frequency

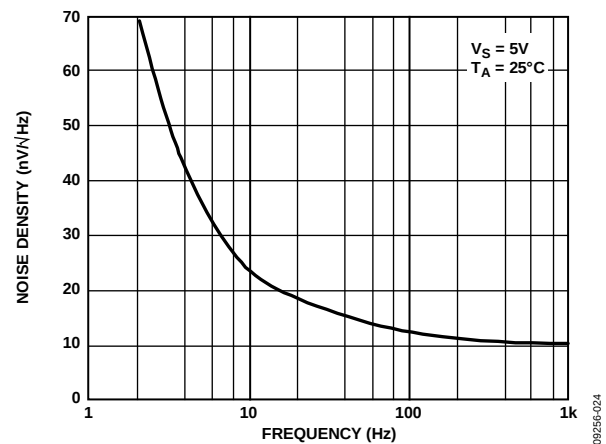


Figure 19. Voltage Noise Density vs. Frequency

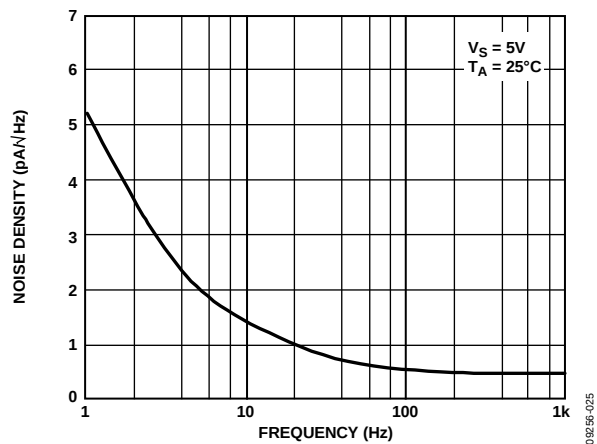


Figure 20. Current Noise Density vs. Frequency

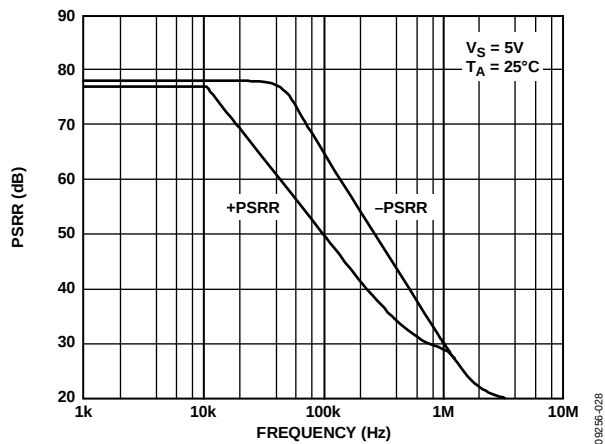


Figure 23. PSRR vs. Frequency

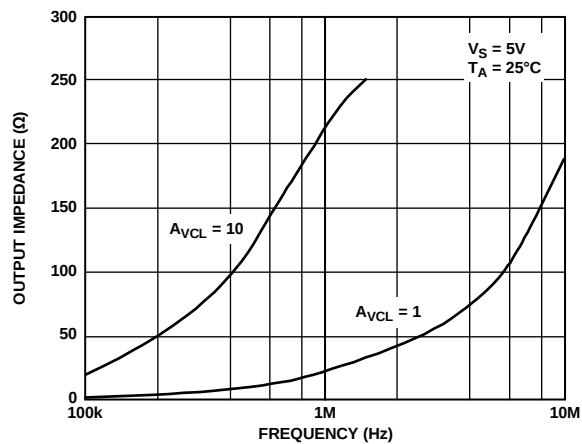


Figure 21. Output Impedance vs. Frequency

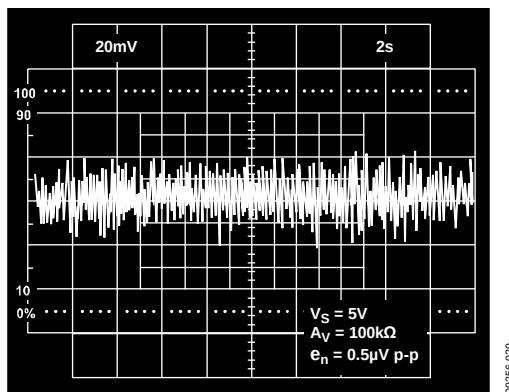


Figure 24. 0.1 Hz to 10 Hz Noise

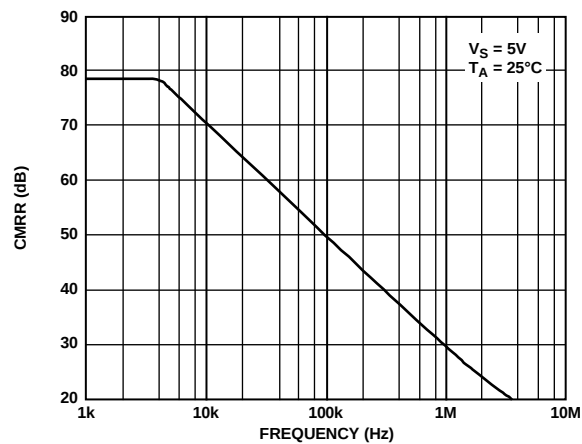


Figure 22. CMRR vs. Frequency

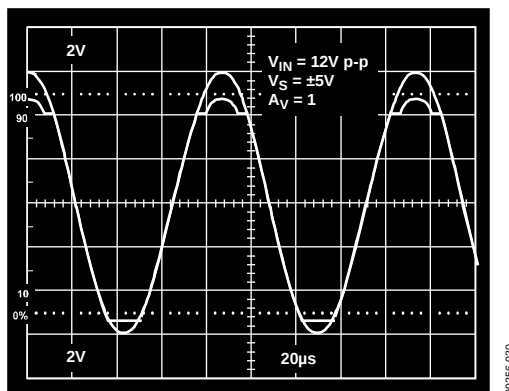
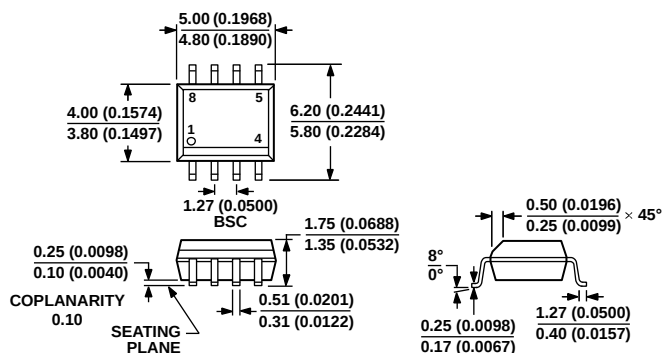


Figure 25. No Phase Reversal ($V_{IN} = 12V$ p-p, $V_S = \pm 5V$, $A_V = 1$)

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 26. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)

Dimensions shown in millimeters and (inches)

012607-A

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
OP262TRZ-EP	–55°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
OP262TRZ-EP-R7	–55°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8

¹ Z = RoHS Compliant Part.

NOTES