28 V, 99 mΩ, Load Switch with Programmable Current Limit and Slew Rate Control

OPERATION DESCRIPTION

The SiP32430 is a load switch integrates multiple control features that simplify the design and increase the reliability of the circuitry connected to the switch. The SiP32430 is designed to operate in the 6 V to 28 V range.

An internally generated gate drive voltage ensures low switch resistance over the wind input voltage operating range.

The SiP32430 has a slew rate control circuit that programs the switch turn-on time to the value set by an external capacitor.

An over-current protection circuit (OCP) continuously monitors the current through the load switch. When the over current protection is triggered, the circuit controls the switch impedance to clamp the current to the level programmed by an external resistor. The trigger current is typically 8 % over the set current limit. In case the over-current condition persists for more than 7 ms, the switch shuts off automatically.

The SiP32430 has an over temperature protection circuit (OTP) which will shut the switch off immediately if the junction temperature exceeds over temperature limit of typically 150 °C. The OTP circuit will release the switch when the temperature has decreased by about 20 °C of hysteresis.

When an OCP or an OTP fault condition is detected the FLG pin is pulled low. The fault flag will release 150 ms after the fault condition is cleared, and the switch will automatically turn on at the programmed slew rate.

The SiP32430 features a low voltage control logic interface which can be controlled without the need for level shifting. It also includes a power good flag.

The SiP32430 is available in a space efficient DFN10 of 3 mm x 3 mm package.

FEATURES

- 6 V to 28 V operation
- Programmable soft start
- Programmable current limit
- Over temperature protection
- ON resistance 99 mΩ
- Power good, when V_{OUT} reaches 90 % of V_{IN}
- OCP / OTP fault flag
- Under voltage lockout: 4.8 V / 5.4 V (typ. / max.)
- If no OTP, auto re-try to soft turn on 150 ms after the switch protected OFF
- Package: DFN10 3 mm x 3 mm
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb Pb-free

RoHS COMPLIANT

HALOGEN FREE Available

APPLICATIONS

- Personal computers
- Lighting
- Flat panel displays
- Game consoles
- Industrial
- Network communication
- Data storage

TYPICAL APPLICATION CIRCUIT

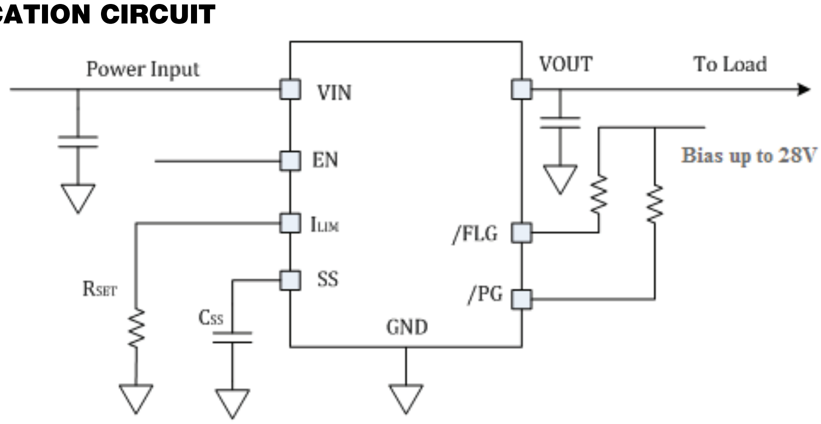

Fig. 1 - SiP32430 Typical Application Circuit

ORDERING INFORMATION			
TEMPERATURE RANGE	PACKAGE	MARKING	PART NUMBER
-40 °C to +85 °C	DFN10 3 mm x 3 mm	2430	SiP32430DN-T1-GE4

Note

- GE4 denotes halogen-free and RoHS-compliant

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	**LIMIT**	**UNIT**
Input Voltage (V_{IN})	-0.3 to 30	V
Output Voltage (V_{OUT})	-0.3 to V_{IN} + 0.3 V	
$\overline{PG}$ Voltage	-0.3 to 30	
$\overline{FLG}$ Voltage	-0.3 to 30	
EN Voltage	-0.3 to 6	
Maximum Continuous Switch Current	3.2	A
ESD Rating (HBM)	4000	V
Maximum Junction Temperature	150	°C
Storage Temperature	-55 to +150	
Thermal Resistance ($_{thJA}$) [a]	88	°C/W
Power Dissipation (P_D) [a, b]	1.42	W

Notes

a. Device mounted with all lead and power pad soldered or welded to PCB.
b. Derate 11.4 mW/°C above T_A = 25 °C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE		
PARAMETER	**LIMIT**	**UNIT**
Input Voltage (V_{IN})	6 to 28	V
V_{SS}	0 to 6	
V_{OUT}	0 to 28	
EN	0 to 6	
$\overline{FLG}$. $\overline{PG}$	0 to V_{IN}	
I_{LIM}	0 to 6	
Current Limit	0.1 to 1	A
Operating Temperature Range	-40 to +85	°C

SPECIFICATIONS							
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS SPECIFIED V_{IN} = 12 V, V_{EN} = 2.4 V, T_A = 25 °C	TEMP.	MIN.	TYP.	MAX.	UNIT
Power Input Voltage	V_{IN}		-	6	-	28	V
Quiescent Current	I_Q	I_{OUT} = 0 A, and device enabled	-	-	163	300	µA
Shutdown Current	I_{SD}	I_{OUT} = 0 A, and device disabled	-	-	11	20	
Switch OFF Leakage	$I_{(OFF)}$	V_{IN} = 28 V, V_{OUT} = 0 V (current measured at output)	-	-	-	1	
Current Limit Clamp		R_{SET} = 12 kΩ	-40 °C to +85 °C	0.28	0.35	0.42	A
Current Limit Trigger		% above setting current	-40 °C to +85 °C	-	8	-	%
Switch ON Resistance	$R_{DS(on)}$	I_{SW} = 500 mA	-	-	99	120	mΩ
Soft Start Charge Current	I_{SS}	Constant current source	-	-	4.5	-	µA
Turn ON Delay Time	T_{ON_DLY}	50 % V_{EN} to 50 % V_{OUT}, C_{SS} = open, R_L = 10 Ω, C_{OUT} = 10 µF	-	-	0.8	-	ms
		50 % V_{EN} to 50 % V_{OUT}, C_{SS} = 47 nF, R_L = 10 Ω, C_{OUT} = 10 µF	-	-	6.7	-	
Turn ON Rise Time	T_R	C_{SS} = open, R_L = 10 Ω, C_{OUT} = 10 µF	-	-	1	-	
		C_{SS} = 47 nF, R_L = 10 Ω, C_{OUT} = 10 µF	-	-	9.5	-	
		C_{SS} = 47 nF, no R_L, C_{OUT} = 10 µF	-	-	2.5	-	
Turn OFF Delay	T_{OFF_DLY}		-	-	8	-	µs
Current Limit Response Time			-	-	20	-	
Short Circuit Response Time			-	-	1	-	
OC Flag Blanking Time / Switch OFF delay under OC			-40 °C to +85 °C	4	-	-	ms
Auto re-try time			-	-	150	-	
Input Logic High Voltage	V_{ENH}	V_{IN} = 6 V to 28 V	-40 °C to +85 °C	1.5	-	-	V
Input Logic Low Voltage	V_{ENL}		-40 °C to +85 °C	-	-	0.6	
Input Pull Down Resistor	R_{EN}	V_{EN} = 5 V	-	-	2.5	-	MΩ
Power Good Trip Voltage			-	-	90 % x V_{IN}	-	V
Power Good Hysteresis			-	-	3 % x V_{IN}	-	
$\overline{PG}$ and $\overline{FLG}$ Output Logic Low Voltage		I_{SINK} = 1 mA	-	-	< 0.1	-	
$\overline{PG}$ and $\overline{FLG}$ Output High Leakage		V_{PG}, V_{FLG} = 28 V	-	-	-	1	µA
UVLO Threshold			-	-	4.8	5.4	V
UVLO Hysteresis			-	-	0.28	-	
Thermal Shut-down Threshold			-	-	150	-	°C
Thermal Shut-down Hysteresis			-	-	20	-	

TIMING DIAGRAM

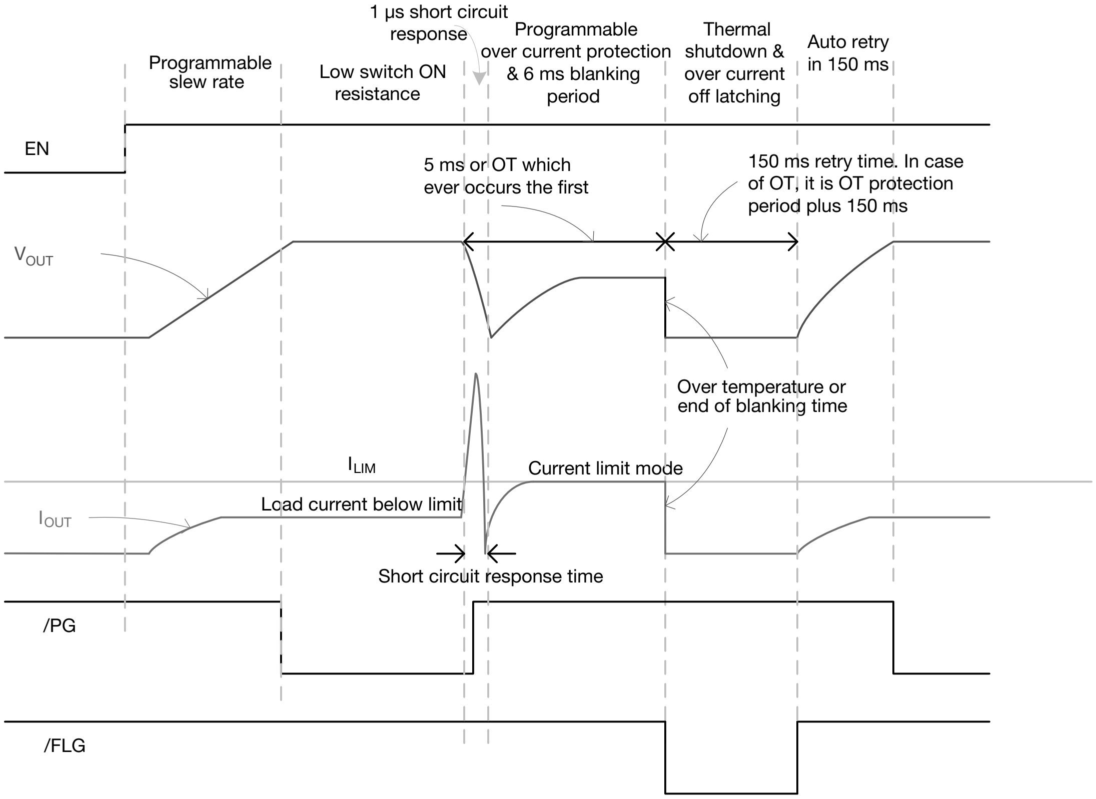

Fig. 2 - Timing Diagram

PIN CONFIGURATION

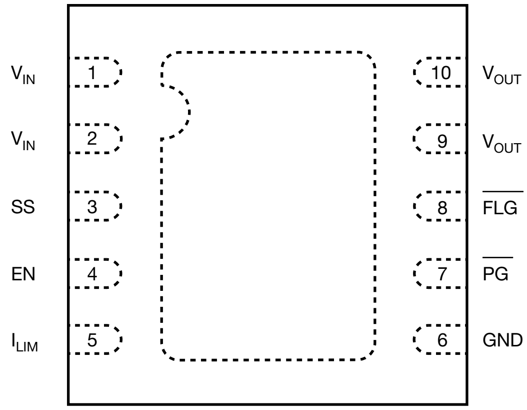

Fig. 3 - DFN10 3 mm x 3 mm Package
Top View

PIN DESCRIPTION		
PIN NUMBER	**NAME**	**FUNCTION**
1	V_{IN}	Power input
2	V_{IN}	Power input
3	SS	Soft-Start pin. Connect a capacitor from SS to GND to program the soft-start time. Leave SS open to set the default soft-start time of 400 μs.
4	EN	Enable input. Logic high enabled
5	I_{LIM}	Current limit setting pin. Connect R_{SET} resistor to GND
6	GND	Ground
7	$\overline{PG}$	Power Good
8	$\overline{FLG}$	Fault condition flag
9	V_{OUT}	Switch output
10	V_{OUT}	Switch output
Central Pad		Connect this pad to GND or leave it floating

BLOCK DIAGRAM

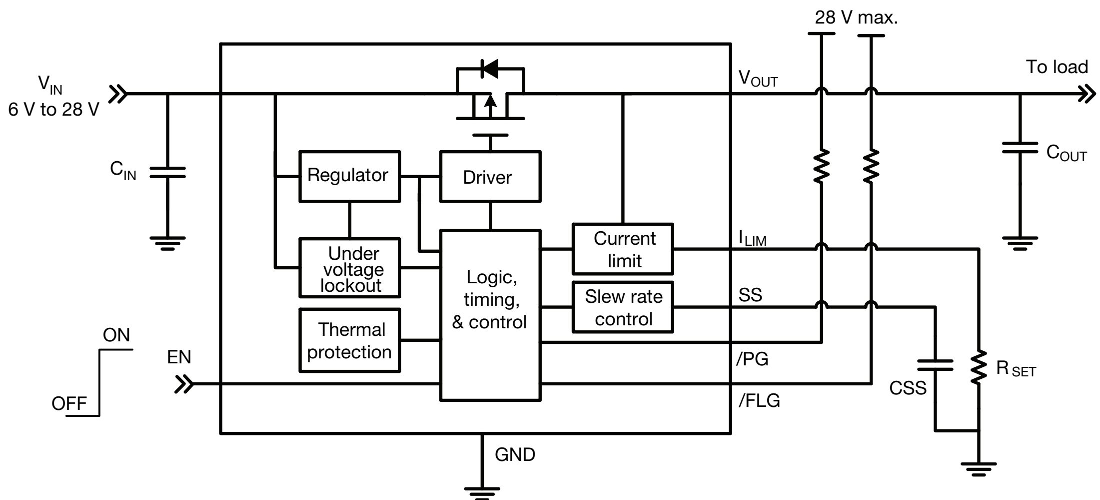

Fig. 4 - Block Diagram

TYPICAL CHARACTERISTICS (internally regulated, 25 °C, unless otherwise noted)

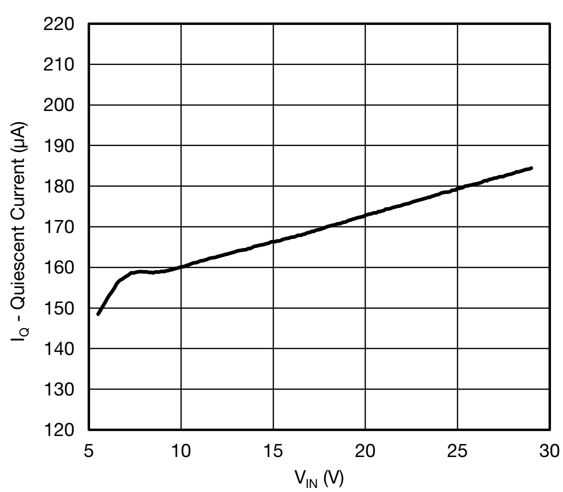

Fig. 5 - Quiescent Current vs. Input Voltage

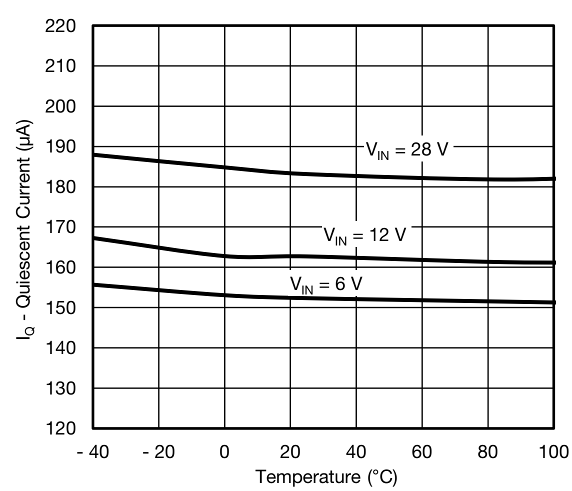

Fig. 6 - Quiescent Current vs. Temperature

TYPICAL CHARACTERISTICS (internally regulated, 25 °C, unless otherwise noted)

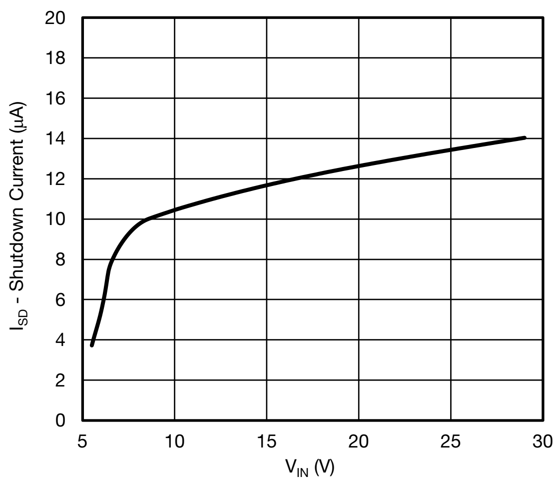

Fig. 7 - Shutdown Current vs. Input Voltage

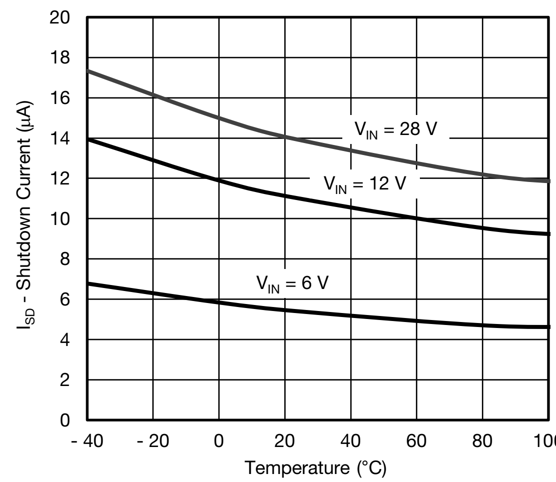

Fig. 10 - Shutdown Current vs. Temperature

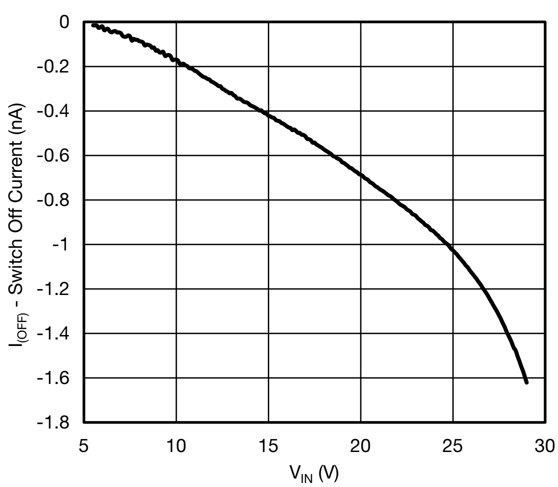

Fig. 8 - Shutdown Current vs. Input Voltage

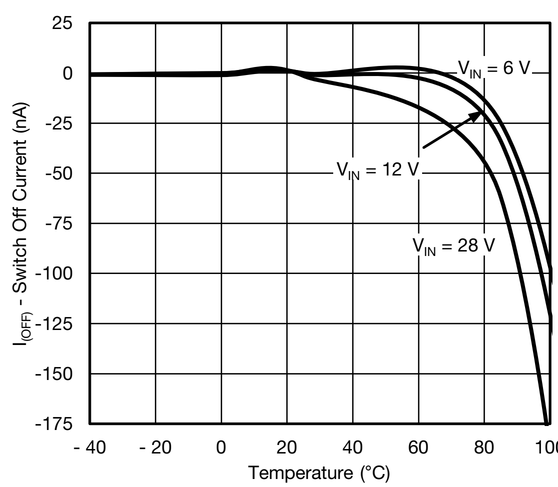

Fig. 11 - Switch OFF Current vs. Temperature

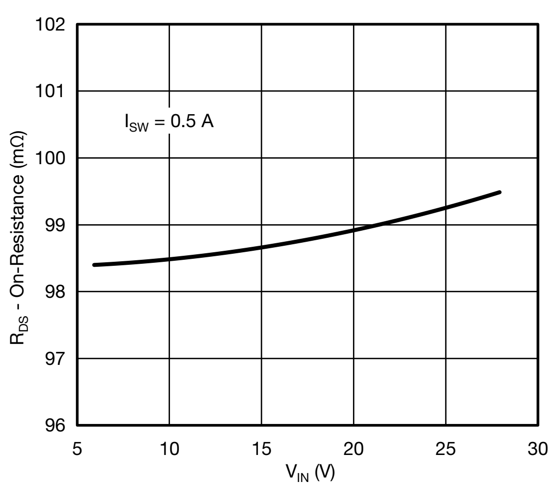

Fig. 9 - ON Resistance vs. Input Voltage

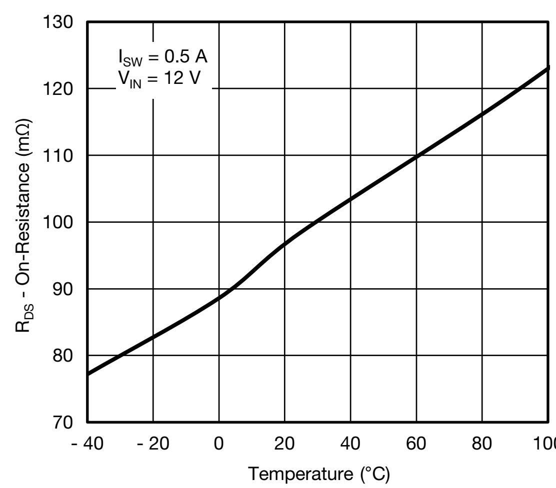

Fig. 12 - ON Resistance vs. Temperature

TYPICAL CHARACTERISTICS (internally regulated, 25 °C, unless otherwise noted)

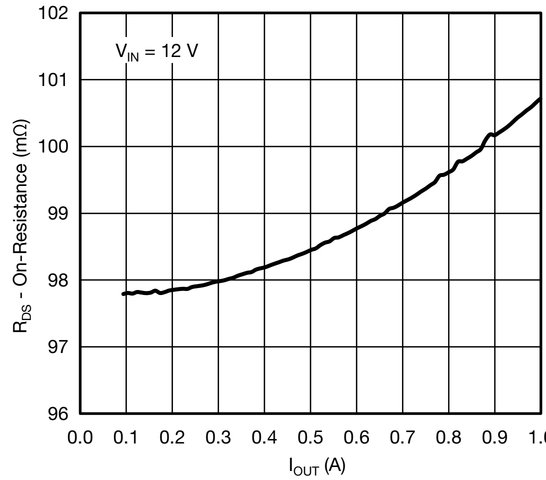

Fig. 13 - ON Resistance vs. Output Current

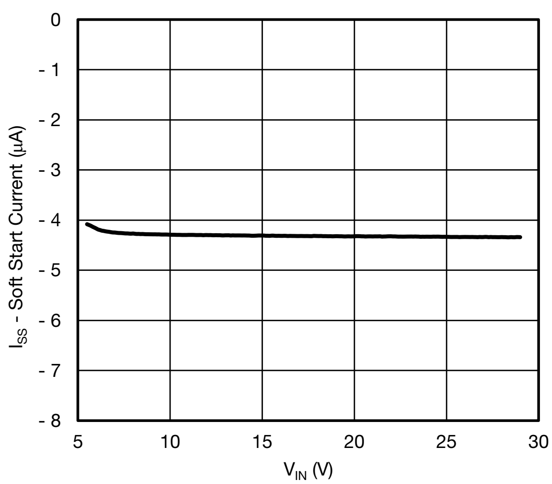

Fig. 14 - Soft Start Current vs. Input Voltage

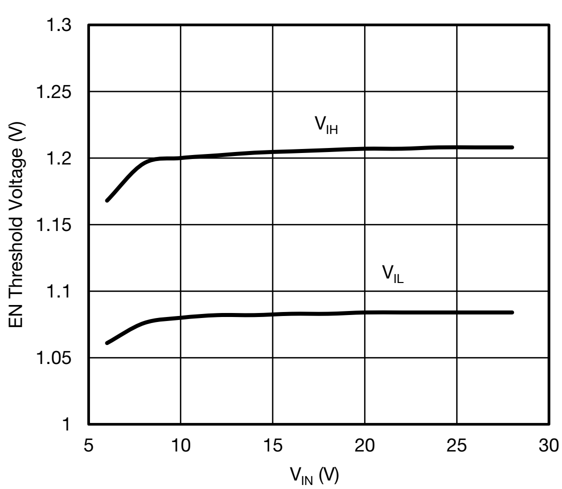

Fig. 15 - Threshold Voltage vs. Input Voltage

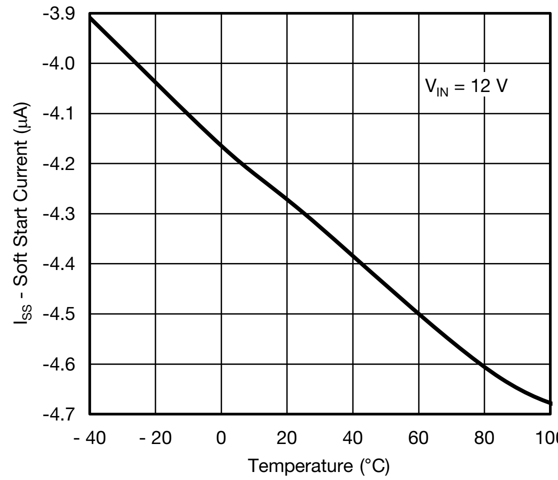

Fig. 16 - Soft Start Current vs. Temperature

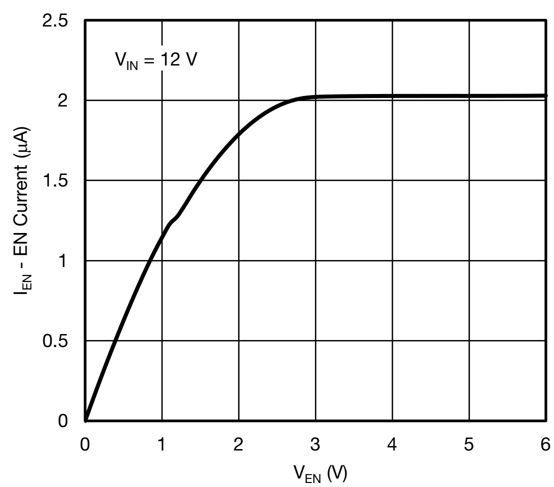

Fig. 17 - EN Current vs. V_{EN}

TYPICAL CHARACTERISTICS (internally regulated, 25 °C, unless otherwise noted)

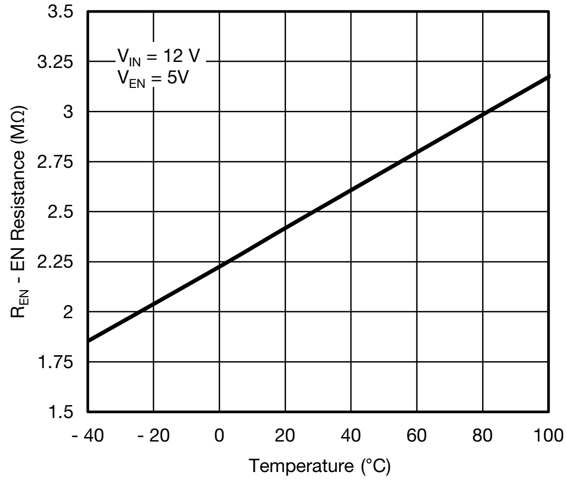

Fig. 18 - EN Resistance vs. Temperature

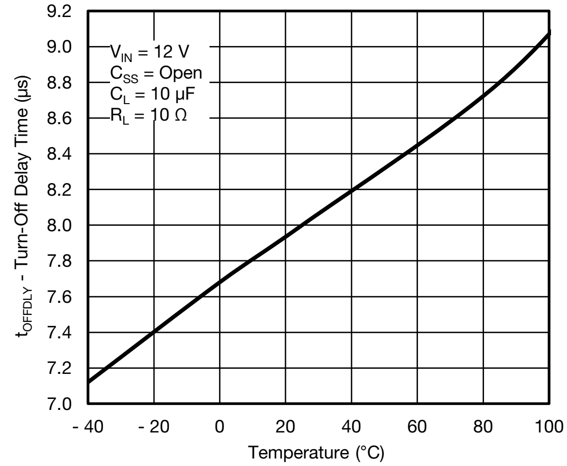

Fig. 21 - Turn-OFF Delay Time vs. Temperature

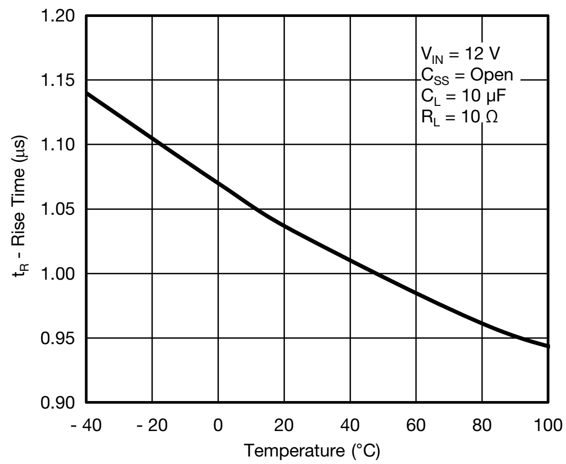

Fig. 19 - Rise Time vs. Temperature

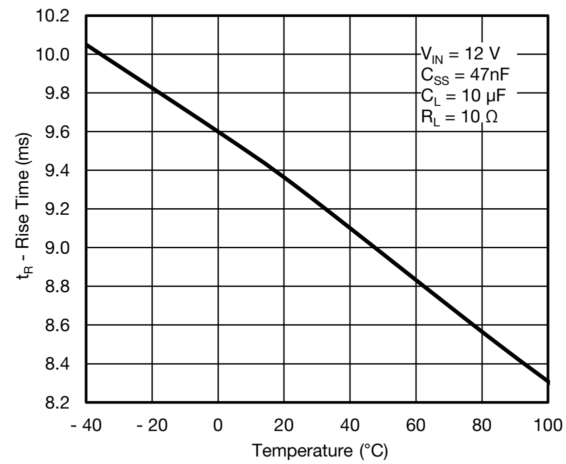

Fig. 22 - Rise Time vs. Temperature

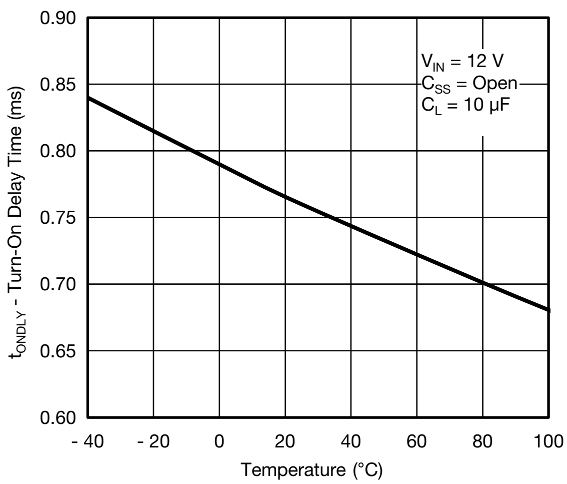

Fig. 20 - Turn-ON Delay Time vs. Temperature

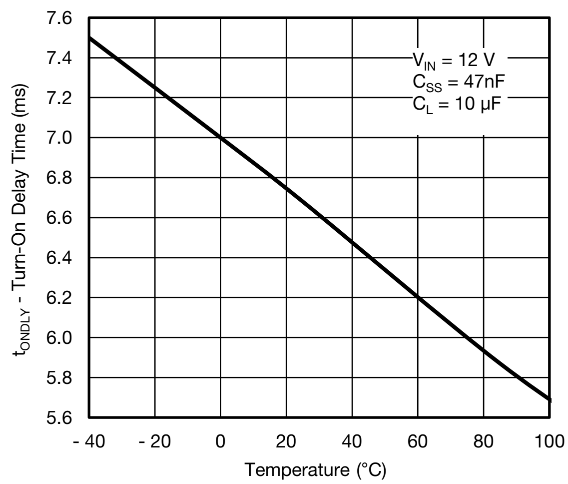

Fig. 23 - Turn-ON Delay Time vs. Temperature

TYPICAL WAVEFORMS

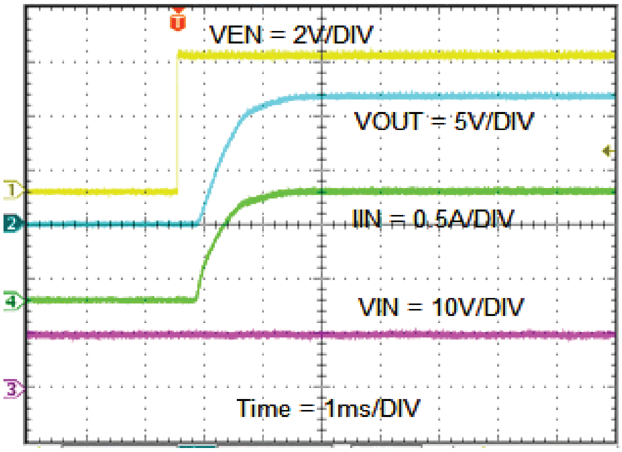

Fig. 24 - Turn-ON Time,
V_{IN} = 12 V, C_{SS} = open, R_L = 10 Ω, C_L = 10 µF

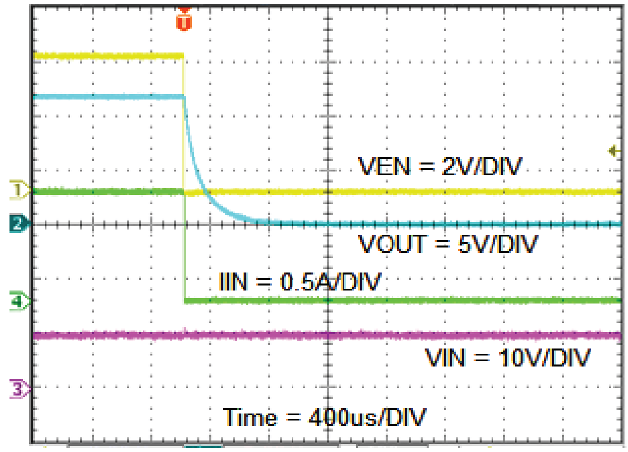

Fig. 27 - Turn-OFF Time,
V_{IN} = 12 V, C_{SS} = open, R_L = 10 Ω, C_L = 10 µF

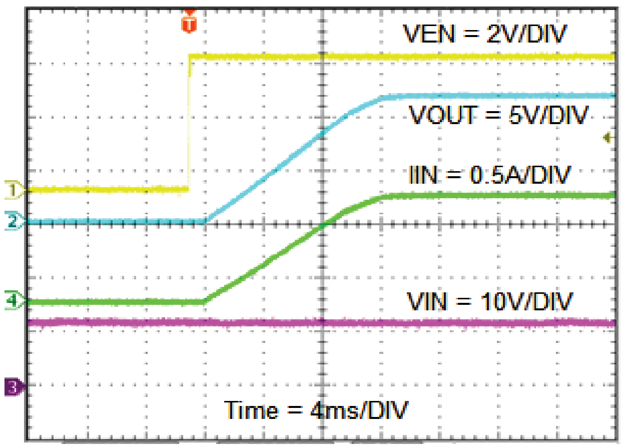

Fig. 25 - Turn-ON Time,
V_{IN} = 12 V, C_{SS} = 47 nF, R_L = 10 Ω, C_L = 10 µF

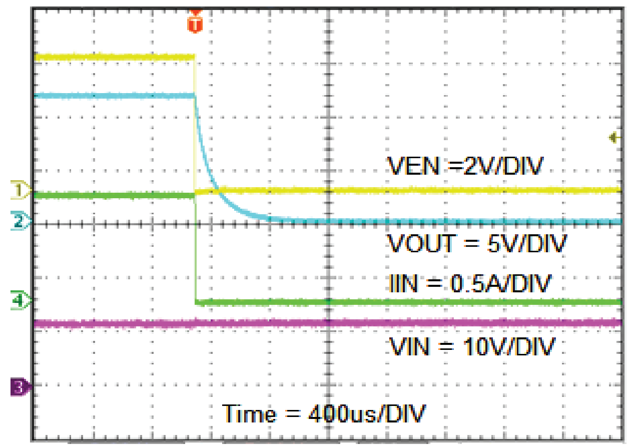

Fig. 28 - Turn-OFF Time,
V_{IN} = 12 V, C_{SS} = 47 nF, R_L = 10 Ω, C_L = 10 µF

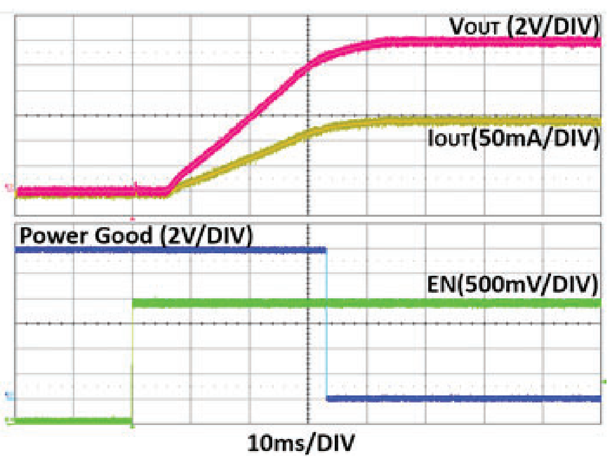

Fig. 26 - V_{IN} = 12 V, R_L = 82 Ω, R_{SET} = 16.2 kΩ,
C_{ss} = 150 nF, C_{OUT} = open

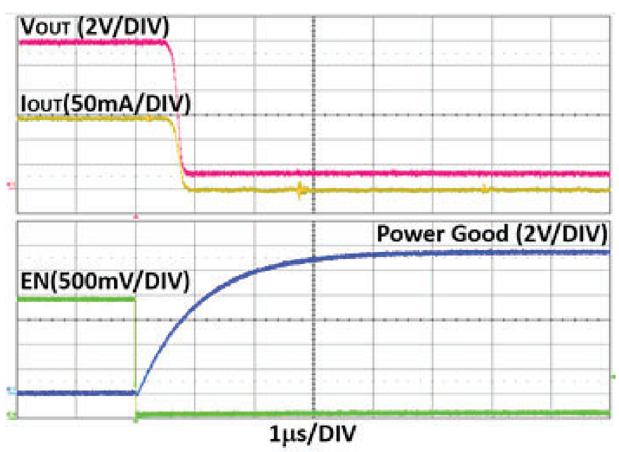

Fig. 29 - V_{IN} = 12 V, R_L = 82 Ω, R_{SET} = 16.2 kΩ,
C_{ss} = 150 nF, C_{OUT} = open

TYPICAL WAVEFORMS

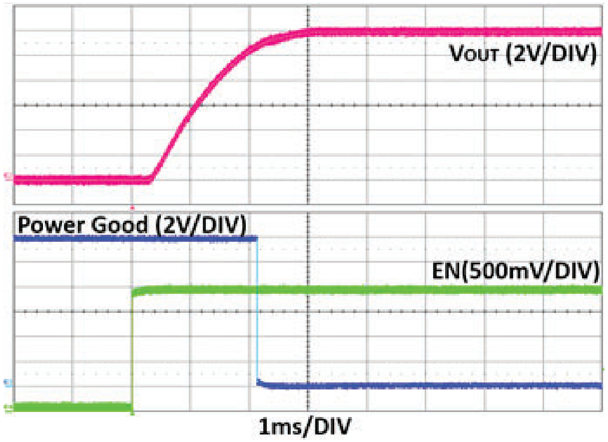

Fig. 30 - V_{IN} = 12 V, R_L = open, R_{SET} = 16.2 kΩ, C_{ss} = 150 nF, C_{OUT} = open

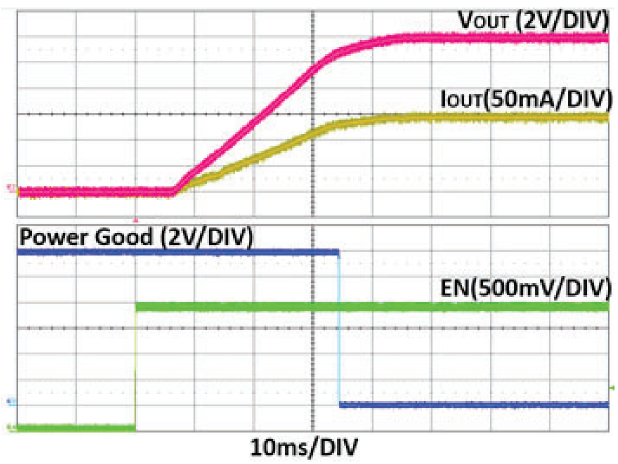

Fig. 31 - V_{IN} = 12 V, R_L = 82 Ω, R_{SET} = 16.2 kΩ, C_{ss} = 150 nF, C_{OUT} = 10 µF

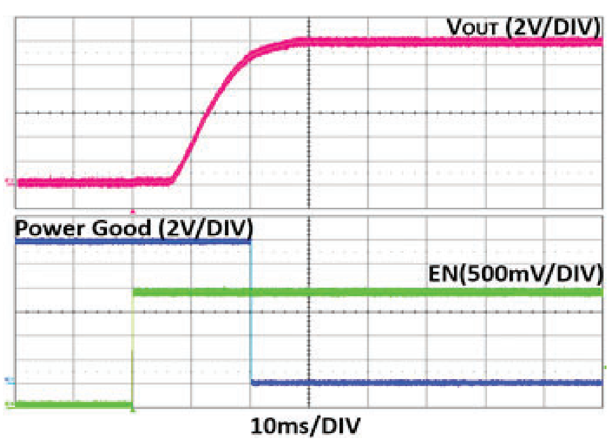

Fig. 32 - V_{IN} = 12 V, R_L = open, R_{SET} = 16.2 kΩ, C_{ss} = 150 nF, C_{OUT} = 10 µF

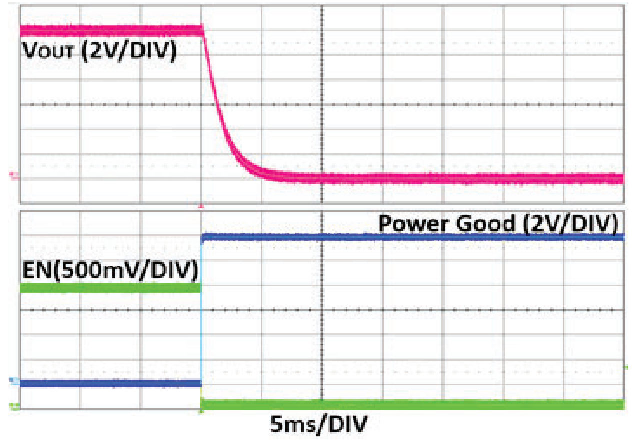

Fig. 33 - V_{IN} = 12 V, R_L = open, R_{SET} = 16.2 kΩ, C_{ss} = 150 nF, C_{OUT} = open

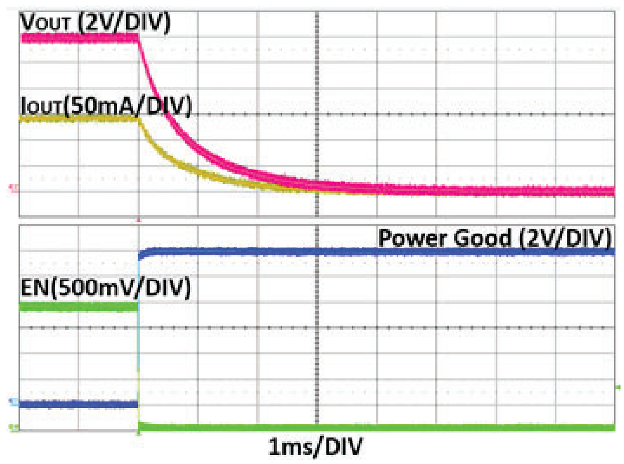

Fig. 34 - V_{IN} = 12 V, R_L = 82 Ω, R_{SET} = 16.2 kΩ, C_{ss} = 150 nF, C_{OUT} = 10 µF

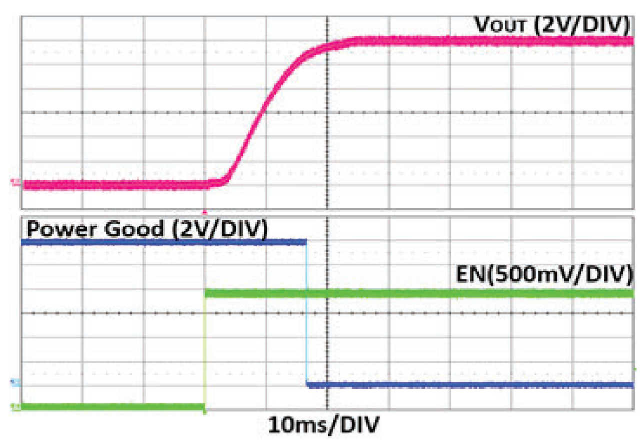

Fig. 35 - V_{IN} = 12 V, R_L = open, R_{SET} = 3.32 kΩ, C_{ss} = 150 nF, C_{OUT} = 10 µF

TYPICAL WAVEFORMS

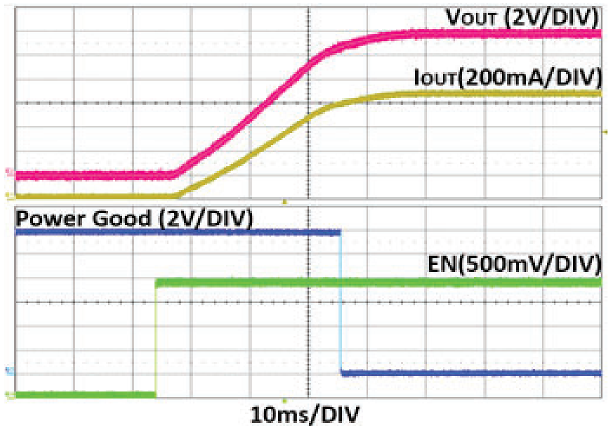

Fig. 36 - V_{IN} = 12 V, R_L = 14 Ω, R_{SET} = 3.32 kΩ, C_{ss} = 150 nF, C_{OUT} = open

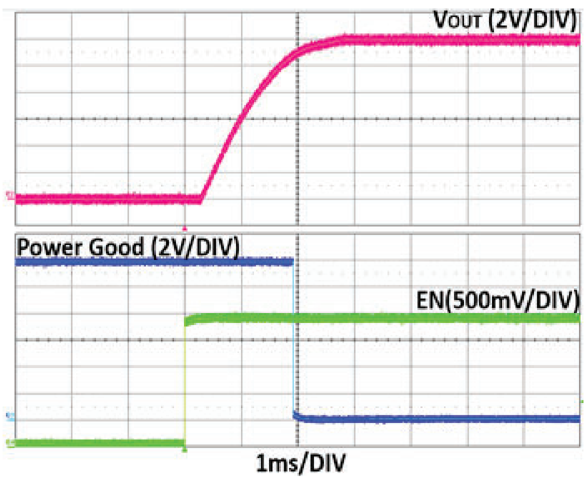

Fig. 37 - V_{IN} = 12 V, R_L = open, R_{SET} = 3.32 kΩ, C_{ss} = 150 nF, C_{OUT} = open

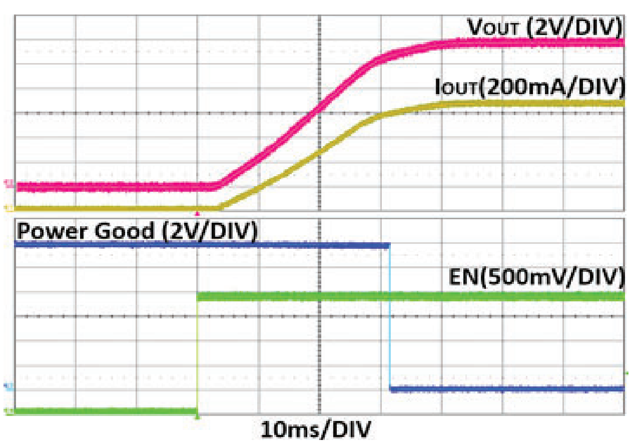

Fig. 38 - V_{IN} = 12 V, R_L = 14 Ω, R_{SET} = 3.32 kΩ, C_{ss} = 150 nF, C_{OUT} = 10 µF

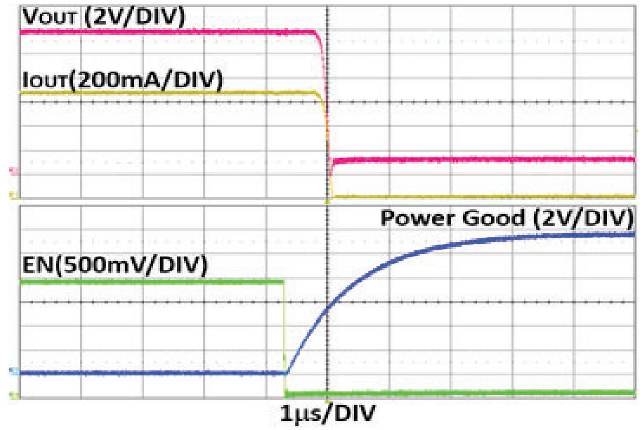

Fig. 39 - V_{IN} = 12 V, R_L = 14 Ω, R_{SET} = 3.32 kΩ, C_{ss} = 150 nF, C_{OUT} = open

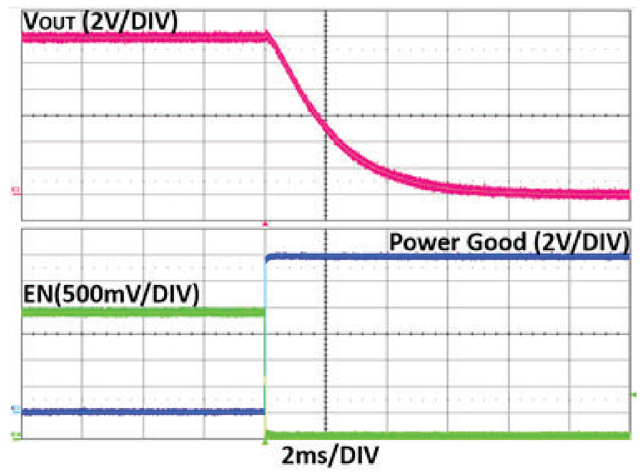

Fig. 40 - V_{IN} = 12 V, R_L = open, R_{SET} = 3.32 kΩ, C_{ss} = 150 nF, C_{OUT} = open

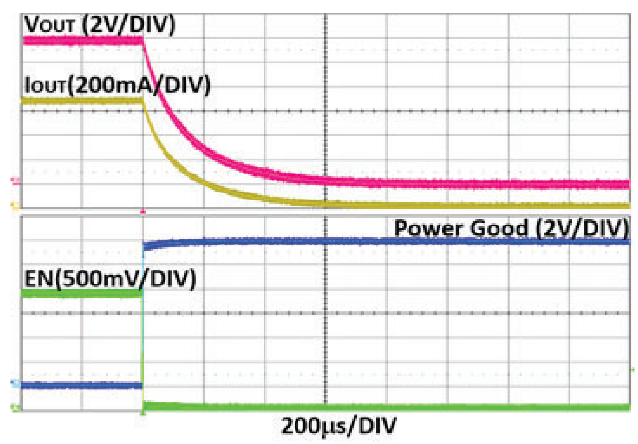

Fig. 41 - V_{IN} = 12 V, R_L = 14 Ω, R_{SET} = 3.32 kΩ, C_{ss} = 150 nF, C_{OUT} = 10 µF

TYPICAL WAVEFORMS

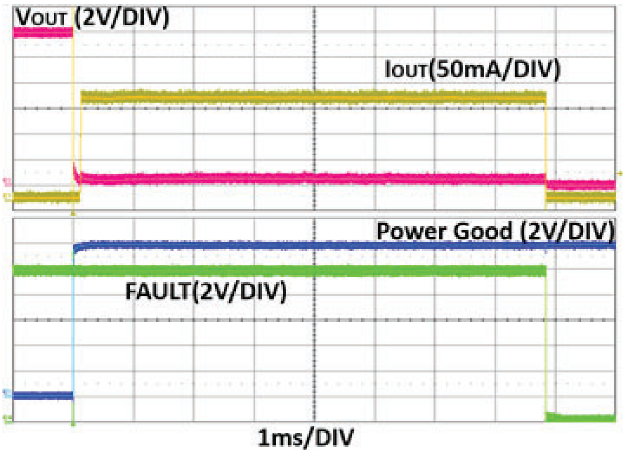

Fig. 42 - V_{IN} = 12 V, R_L = open to 2 Ω, R_{SET} = 16.2 kΩ, C_{ss} = 150 nF, C_{OUT} = open

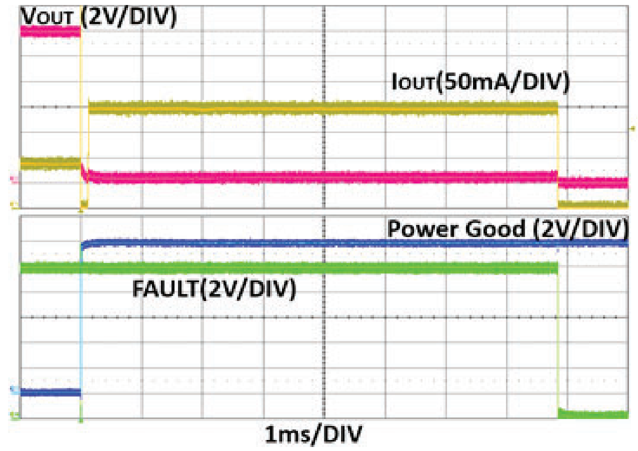

Fig. 45 - V_{IN} = 12 V, R_L = 136 Ω to 2 Ω, R_{SET} = 16.2 kΩ, C_{ss} = 150 nF, C_{OUT} = open

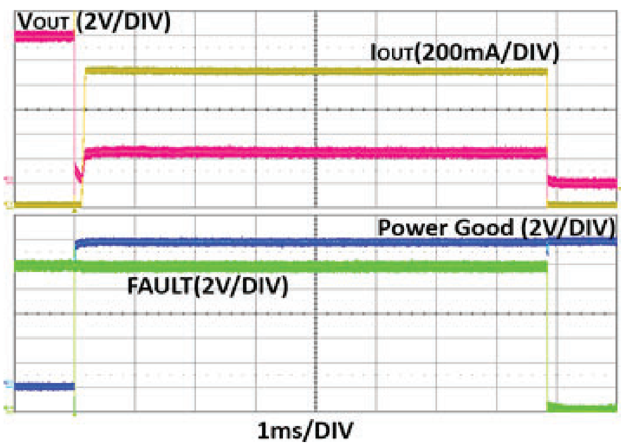

Fig. 43 - V_{IN} = 12 V, R_L = open to 2 Ω, R_{SET} = 3.32 kΩ, C_{ss} = 150 nF, C_{OUT} = open

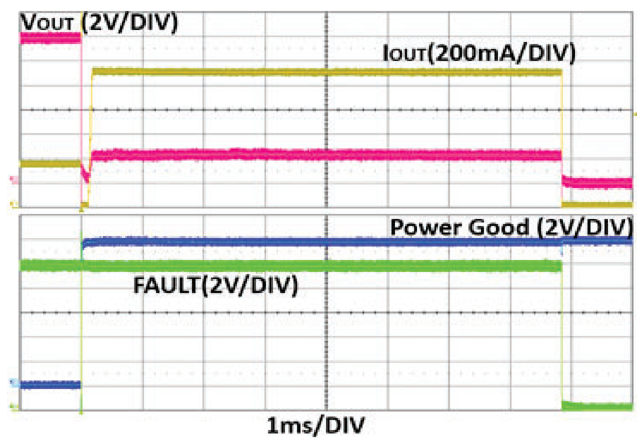

Fig. 46 - V_{IN} = 12 V, R_L = 34 Ω to 2 Ω, R_{SET} = 3.32 kΩ, C_{ss} = 150 nF, C_{OUT} = open

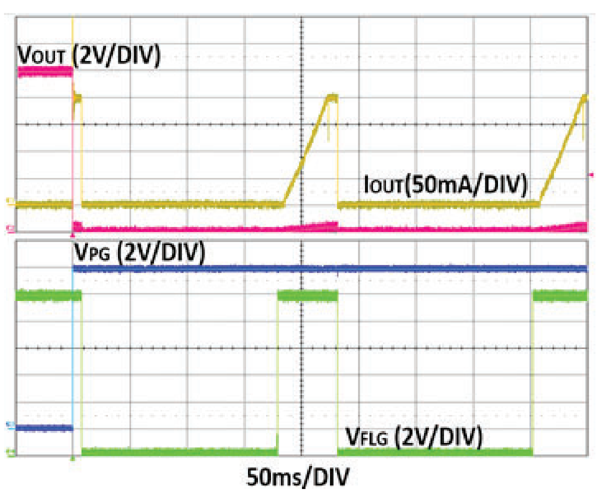

Fig. 44 - V_{IN} = 12 V, R_L = 2 Ω, R_{SET} = 16.2 kΩ, C_{ss} = 150 nF, C_{OUT} = 10 µF, Re-Starts after ~ 150 ms during Fault Condition

DETAILED DESCRIPTION

Over Current Limit

When an over-current event occurs, the SiP32430 will limit the current immediately. If the event exceeds 7 ms, the SiP32430 will turn off the switch. The $\overline{FLG}$ pin is pulled low upon the switch off. The SiP32430 will auto restart 150 ms after the switch off and the recovery from over temperature. The SiP32430 current limit is set an external resistor between the I_{LIM} pin and GND. R_{SET} can be selected per the following table and curve.

R_{SET} SELECTION TABLE

R_{SET} (kΩ)	CURRENT LIMIT (A) (SETTLING)			TOL. (%)	CURRENT LIMIT TRIGGER POINT (A)
	MIN.	TYP.	MAX.		TYP.
4.22	0.81	1.01	1.21	20	1.12
5.36	0.65	0.81	0.97	20	0.87
7.15	0.49	0.61	0.73	20	0.66
10.2	0.33	0.42	0.50	20	0.46
12	0.28	0.35	0.42	20	0.38
13.3	0.25	0.31	0.37	20	0.35
18.7	0.17	0.21	0.26	20	0.25
24.3	0.11	0.16	0.21	30	0.19

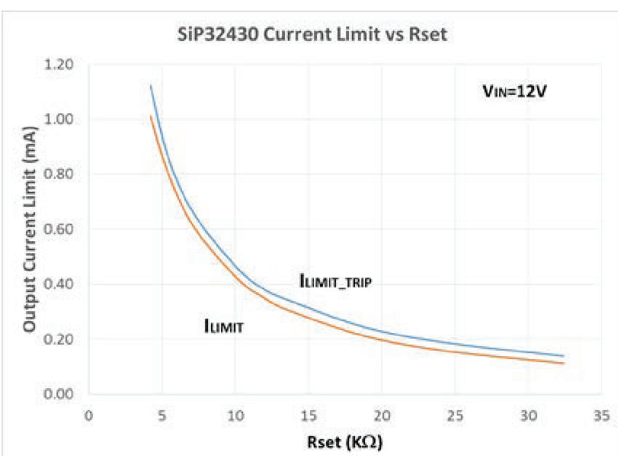

Fig. 47 - Current Limit vs. R_{SET}

The current limit trigger level is typically 8 % over the current limit setting current.

Soft Start

The soft start time can be calculated by the following formula:

$$\frac{\Delta V_{OUT}}{\Delta t} = \frac{I_{SS}}{C_{SS}} \times \frac{R_{OUT} \times 3300}{R_{SET}}$$

Where:
Δt is the soft start time
ΔV_{OUT} is the output voltage range
I_{SS} is the built-in current source charging the soft start capacitor C_{SS}. I_{SS} value is 5 µA typical.
C_{SS} is the soft start time setting capacitor.
R_{SET} is the current limit setting resistor.
R_{OUT} is the output load.

Enable

The device is logic high enable. This can be accomplished by applying a logic high signal to the EN pin. Alternatively this pin can be hardwired through a resistor divider to the V_{IN}, thus keeping the switch permanently ON as long as the supply is present.

$\overline{FLG}$

The $\overline{FLG}$ is an open drain output and will be pulled low under over temperature or over current conditions.

$\overline{PG}$

The $\overline{PG}$ is an open drain output that will be pulled low when output voltage reaches 90 % of the V_{IN}.

APPLICATION INFORMATION

Input Capacitor

While bypass capacitors at the inputs pins are not required, a 2.2 µF or larger capacitors for C_{IN} is recommended in almost all applications. The bypass capacitors should be placed as physically close to the device's input pins to be effective to minimize transients on the input. Ceramic capacitors are recommended over tantalum because of their ability to withstand input current surges from low impedance sources such as batteries.

Output Capacitor

SiP32430 does not require an output capacitor for proper operation. A proper value C_{OUT} is recommended to accommodate load transient per circuit design requirements. There are no specific ESR or capacitor type requirements.

Over Temperature Shutdown

In case an over temperature event happens, the SiP32430 will turn the switch off immediately. The SiP32430 will then retry to start 150 ms after the temperature is back to normal; during this period, $\overline{FLG}$ will be pulled low. The SiP32430 $\overline{FLG}$ will be pulled high 150 ms after the OT event has finished.

Thermal Consideration

SiP32430 is designed to maintain a constant output load current under over current event. Due to physical limitations of the layout and assembly of the device, the maximum switch current should be kept at reasonably safe level within the range of SOA. However, another limiting characteristic of the safe operating load current is the power dissipation. The power dissipation need to be considered in the layout design to reduce the device temperature.

SOA

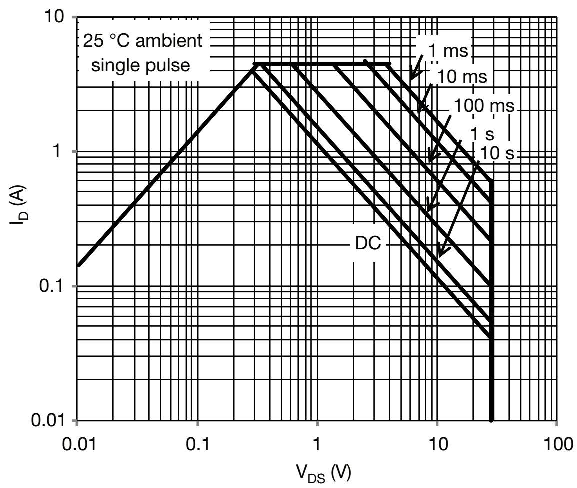

Fig. 48 - SOA on Application Board

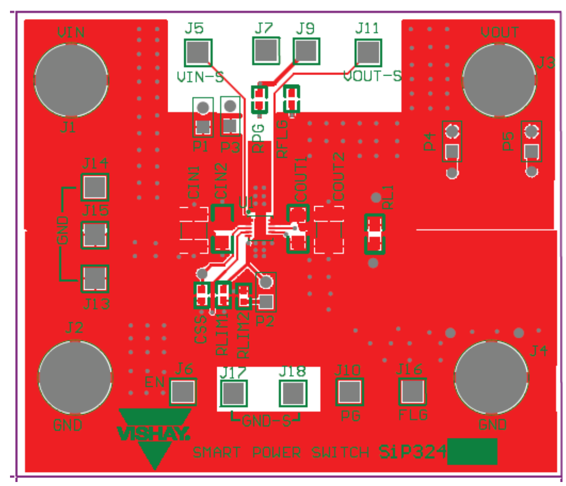

Fig. 49 - Application Board Layout

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